Recent processing advances towards full-wafer two-terminal perovskite/silicon tandem solar cells

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Abstract

Two-terminal tandem solar cells based on perovskite/silicon (PK/Si) technology represent one of the most exciting pathways towards pushing solar cell efficiencies beyond the thermodynamic limit of single-junction crystalline silicon devices. While laboratory efficiencies of these tandem cells have risen to very impressive levels, many important innovations towards enabling their eventual manufacturability have also been made in this rapidly evolving field. In this paper, a number of these processing innovations are highlighted in order to give a more complete view as to the viability of scaling up the processing of these devices. Specifically, the focus is placed on how today's crystalline silicon process flows could be adapted in order to allow existing cell lines to produce PK/Si cells. Additionally, the adoption of new processes for deposition of the perovskite subcell is also examined. The discussion of these innovations aims to spotlight the significant advances in this field, but also to highlight many of the future manufacturing challenges that this technology will face.

Introduction

Over the last few decades, the cost of PV energy systems has plummeted, with massive reductions in overall system cost on a dollar per watt basis [1]. This reduction in cost has been partially driven by significant improvements in overall module power conversion efficiency. At the heart of this improvement has been the deployment and optimization of new crystalline silicon cell technologies, which have been successful in pushing module efficiency ever higher. Today, the industry is getting ready for the large-scale roll-out of silicon heterojunction (HJT) cells, as well as cells based on high-temperature passivating contact (HTPC) structures [2]. With these technologies, a number of companies have realized wafer-level efficiencies of over 25% [3,4]. Such values are gradually approaching the practical limits of single-junction silicon PV [5].

As these technologies are being scaled up in production, research interests have been shifting towards the next technology to push device efficiencies even further, and hopefully continue the gradual reduction in the levelized cost of PV electricity. For the moment, most of this hope rests on the development of a tandem solar cell based on metal-halide perovskite materials on top of a crystalline silicon wafer in a two-terminal configuration (PK/Si tandem structure). Laboratory-sized devices (~1cm^2) based on these structures have shown remarkable progress over the past seven or eight years, with the current world-record devices sitting at an impressive 29.8% efficiency [6].

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While this efficiency is certainly a remarkable achievement, it is perhaps not the most interesting development in the technology. A survey of the literature reveals an astounding diversity in the variety of PK/Si device structures which can exceed the highest both-side-contacted single-junction crystalline silicon device (at an efficiency of 26.3% [7]). This diversity includes different cell polarities (NIP [8] vs. PIN), bottom cell technologies (both HJT and HTPC [9]), bottom cell surface texture (planar, pyramidal, microtextured) and perovskite deposition techniques (spin coating, meniscus coating [10], hybrid deposition [11], and co-evaporation [12]). Such diversity in efficient device structures is unprecedented among thin-film technologies and suggests a tremendous degree of freedom in designing high-efficiency tandem devices.

As a result of the rapid pace of development in the field, as well as the clear potential for extremely high-efficiency devices, the solar cell industry has begun to invest in research, and most major PV manufacturers are now placing PK/Si technology somewhere on their research roadmaps. Although there are certainly still many challenges to overcome for this technology, mostly around the question of device stability and defect control, the question of manufacturability is now relevant for solar cell producers looking to incorporate this technology into their own lines.

In this paper, some recent advances in the scale-up of two-terminal PK/Si tandem devices will be discussed and evaluated. Specifically, the focus will be on looking at the challenges of transferring current high-efficiency laboratory devices to full-wafer devices that could be compatible with current manufacturing processes. This paper will aim to give a perspective on the state of the field rather than a comprehensive review of all the progress that has been made in this area. In addition, the discussion will centre exclusively on two-terminal PK/Si structures rather than including four-terminal-type

devices. Four-terminal tandem technology does have various advantages over two-terminal structures. Nevertheless, a large majority of current crystalline silicon manufacturers are currently devoting their attention to the two-terminal configuration; the discussion in this paper will therefore be limited to this device configuration.

Integration of commercial bottom cells into tandem structures

The most common implementation strategy envisioned for PK/Si tandem manufacturing is that it could be deployed as an upgrade to current cell lines somewhat analogously to how passivated emitter and rear cell (PERC) technology was viewed as an upgrade to aluminium back-surface field (Al-BSF) technology [13]. A simplified version of this would be a modification to existing processing stations to adapt the bottom cells for tandem integration, the addition of several processing stations for deposition of the perovskite sub cell materials, and a subsequent modified back-end process including metallization, interconnection and module lamination.

Modification to silicon solar cells for bottom cell compatibility

When considering an upgrade of an existing crystalline silicon line to a tandem production line, it is worth discussing how a high-performance crystalline silicon solar cell needs to be modified in order to be compatible for tandem integration. Two active developments in this area are: 1) modification of wafer surface texture, and 2) exploration of different bottom cell technologies.

In the area of engineering wafer texture for PK/Si integration, there have been several important advances in the past few years which greatly widen the processing window for the production of these devices. Previously, practically all tandem solar cells were constructed on small float zone (FZ) wafers with a chemically-mechanically polished (CMP) front surface or with a standard pyramidal texture derived from this polished surface. Tandems built on CMP polished wafers benefited from good compatibility with current laboratory deposition methods (i.e. spin coating) for the perovskite absorber layer as well as the contact materials. This allowed a direct transfer of highly optimized deposition recipes from single-junction perovskite solar cell development to tandem solar cells. However, this approach is obviously held back by the unreasonable cost of the CMP process for silicon wafers and is not suitable for industrial production. The other approach, based on a standard pyramidal texture [11], does not have this disadvantage, because this type of texture is the industry standard for monocrystalline silicon solar cells. Be that as it may, this approach is constrained by the need for careful conformal deposition of the perovskite absorber and contact layers, and careful control of the pyramid size and distribution [14]. Despite these constraints, high-efficiency devices have been demonstrated using the pyramidal texture approach [11].

In recent years, two specific advances have been made in the field which greatly enlarge the parameter space for these types of device. First, several groups have demonstrated a technique for fabricating planar tandem solar cells starting from a commercial diamond-wire-cut Czochralski (CZ) wafer [15,16]. This approach relies on wet-chemical polishing of the front surface to remove most of the surface features generated during the wire-sawing process. While this type of chemistry is well known [17], it was unclear whether it could provide sufficient planarization of the wafer surface to be compatible with solution-based perovskite deposition methods. This strategy provides an interesting pathway to achieving planar tandem solar cells using commercial CZ wafers.

The second important advancement in this area has been the fabrication of tandem solar cells using a very small pyramidal texture (microtexture) [18,19]. This method differs significantly from the standard textured approach in that the perovskite layer is deposited so that it effectively planarizes the surface texture by filling in the valleys between the pyramids. Like the chemical planarization approach, this method can exploit well-known wet-chemical etching chemistries for silicon wafers and would, in principle, be compatible with current silicon wet-chemistry processes. The major disadvantage of this technique is the requirement for a fairly long diffusion length in the perovskite layer. Moreover, it remains to be seen how sensitive these kinds of cell are to variations and distributions both in pyramid size across the wafer or between wafer batches and in perovskite thickness. Intriguingly, this method has been shown to be also compatible with potentially scalable perovskite deposition methods based on meniscus coating [19,10].

While neither of these two advances in texture control has yet resulted in record-breaking efficiencies, they are nevertheless important to the field, since they greatly widen the processing window scope for these devices. Specifically, previous arguments about the merits of flat versus fully textured tandems are now less relevant, as it is starting to become clear that intermediate texture devices can now work.

Another important advancement in the modification of crystalline silicon solar cells for tandem applications has been the diversification of the types of bottom cell technology. In the academic literature, most reports on PK/Si tandem solar cells rely on HJT bottom cell technology. The reasons for this are several. First, the high open-circuit voltage and excellent near-infrared (NIR) response of these cells make them an efficient partner in a tandem configuration. On a more practical note, however, these kinds of cell can be prepared fairly quickly in a university/research environment, making them a

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convenient starting point in tandem development.

On the other hand, the vast majority of commercial solar cells (and thus produced cells) are based on PERC solar cells fabricated on p-type wafers. Indeed, a meaningful economic argument can be made for PK/Si tandem solar cells exploiting this existing production capacity [20]. A recent report demonstrated such a tandem solar cell built on a PERC rear side and a poly-Si on oxide (POLO) front side [16]. Although efficiencies are still very low, it is likely that significantly higher efficiencies will be within reach for this tandem configuration.

Beyond HJT and PERC type cells, there have also been meaningful demonstrations of tandem solar cells based upon a HTPC approach [21,22]. Recently, the group at CSEM has pushed this concept further, with the demonstration of a 28.3% 4cm^2 tandem solar cell based on a p-type wafer with HTPCs on both sides [23]. In addition, a collaboration between Qcells and HZB demonstrated a device with 28.7% efficiency based upon Qcells' passivating contact bottom cell technology [9]. It can be seen, on taking a step back, that more and more bottom technologies appear to be adaptable for high-efficiency tandem devices. Again, this agrees with the overall theme of a large processing window for these devices.

Large-area deposition of perovskite layers and contact layers

The deposition of the perovskite absorber and its associated contact layers is perhaps the principal challenge in this field. While there have been many important advances in the upscaling of single-junction perovskite mini-modules [24] in recent years, the same cannot yet be said for PK/Si tandem devices: very few examples of devices beyond several centimetres squared in size have so far been demonstrated. This statement is rather surprising, as the technology for making larger-area bottom cells certainly exists, and an increasing number of researchers have been able to demonstrate impressive efficiencies with single-junction perovskite modules with device areas of several tens of centimetres squared [25–27].

In relation to the above, it is worth highlighting some of the differences in the process and material requirements for a tandem device in comparison to most single-junction devices, which may partially explain this dearth of large-area PK/Si tandems in the literature. These differences can be summarized and placed in three categories:

1) Requirements for thermal stability
2) Tandem-specific bandgap
3) Deposition over rough surfaces

Beginning with thermal stability, a tandem device with perovskite layers must undergo several processing steps that require a certain amount of thermal budget, specifically the buffer layer deposited by atomic layer deposition (ALD), the annealing of a screen-printed Ag paste for the front electrode contact, and the lamination and encapsulation of the module assembly. This thermal budget requirement is not always met by perovskite solar cells, as certain perovskite compositions can be more sensitive to thermal degradation. As a result, these devices must use perovskite compositions with the best thermal stability possible. Practically, what this means is that the simplest perovskite compositions based on the use of a methylammonium cation ($MAPbI_3$) must be replaced with either methylammonium-free or methylammonium-reduced formulations to survive some of these processes [12].

With regard to bandgap, the targeted electronic bandgaps for perovskite materials in a tandem configuration are typically higher than those used in the best single-junction perovskite modules. The need for a higher bandgap and greatly reduced methylammonium content in the perovskite places additional constraints on the perovskite stoichiometries used in tandem devices.

Finally, the deposition surface in a PK/Si tandem will always have some inherent roughness, whether this be a full-size pyramidal texture or a silicon surface after chemical polishing. Even in the case of a chemically polished wafer, this roughness is markedly higher than in single-junction perovskite modules, where the layers are usually deposited on very flat, drawn glass substrates.

In short, what these differences mean is that not all results on a large-area perovskite single-junction device are directly transferable to a PK/Si tandem device.

Even though examples of large-area PK/Si tandems are few and far between, several do exist. In most of these examples, however, the device area is simply increased while still relying on steps, such as spin coating and evaporation of the top metal contact [28,29], that cannot be scaled to a full-size 6" wafer. The group at CSEM has also followed this strategy while incorporating a screen-printed Ag top collection grid to achieve efficiencies of 24.3% on an active area of 57.4cm^2 [30].

Looking beyond such spin-coated devices, only two examples of a relatively large-area PK/Si tandem device which does not use any spin-coating processes were able to be identified. OxfordPV has presented a tandem solar cell with an efficiency of 26.67% over an area of 200cm^2, built on an M6 wafer [31]. Unfortunately, the processes and materials used to achieve this result have not been published. The group at CSEM has also presented details of such a device at the EU PVSEC 2021 conference [32] (Fig. 1). In this example, a PK/Si tandem solar cell was fabricated on a rear emitter HJT on a CZ

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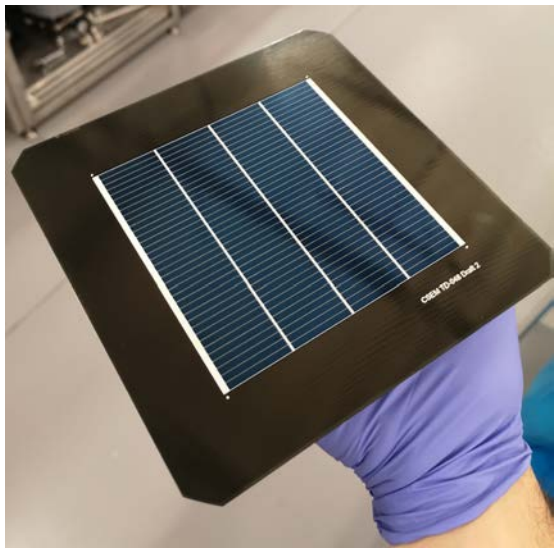

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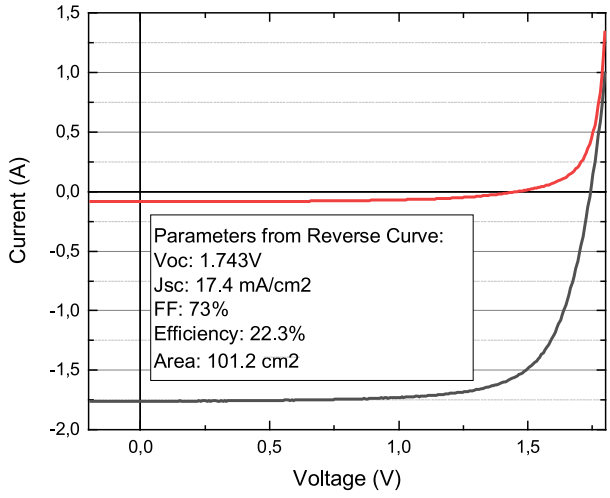

Figure 1. (a) A 101.2cm² PK/Si tandem solar cell built on an M2 HJT bottom cell. (b) *I–V* curve of the record cell with a stabilized efficiency exceeding 22%.

M2 wafer with an active area of 101.2cm². The front side of the wafer was chemically polished to be relatively flat, whereas the rear side was textured to improve the light-trapping efficiency. For the perovskite top cell stack, all the contact layers in that device were deposited by vacuum deposition processes (sputtering, thermal evaporation, ALD), while the perovskite layer itself was deposited using a solution-based blade-coating process and the front metallization was achieved by screen printing a low-temperature Ag paste. The record cell from this experiment yielded an efficiency of 22.3% over an active area of 101.2cm². Despite this efficiency not yet being competitive with a commercial crystalline silicon device, the authors believe that this result is significant for the PK/Si tandem field, as it demonstrates a device using commercial wafers, wet-chemical etching, potentially scalable deposition processes and printable front metallization. In effect, such devices were constructed using a process flow that could potentially be adapted by industry.

Although few examples of large-area PK/Si tandem solar cells have been demonstrated, there have been many groups working on processing technologies which may enable deposition of large-area PK/Si solar cells. Specifically, the past few years have seen several new advances in the scalable deposition of perovskite layers.

One of the fundamental challenges in the scale-up of PK/Si tandem devices is the question of how to deposit the perovskite layer with very high uniformity and high throughput across an entire wafer. One solution which stirred a lot of interest in the industry has been thermal co-evaporation of the perovskite layer directly on a wafer. While co-evaporation of perovskite layers has been known for a relatively long time [33], the successful processing of perovskite layers for PK/Si tandem integration had been lacking from the field until recently. Recent work from a group at HZB showed that this method could be used to create PK/Si tandem devices directly on standard textured bottom cell surfaces, resulting in efficiencies of over 24% [34]. Moreover, several other groups have demonstrated similar methods to produce tandem-appropriate perovskite layers, albeit in single-junction devices [35–37].

These advances are encouraging, but several practical challenges remain with this deposition approach [38]. Primarily, co-evaporation of the perovskite layer remains an extremely slow process, with typical deposition rates of the order of 1–3Å/s. Assuming a 400nm-thick layer, this would result in a processing time of the order of tens of minutes. While some process optimization could be expected, significant improvements to this deposition rate would need to be demonstrated with good repeatability. Related to this challenge is the question of deposition tool design. All examples of thermal co-evaporation in the literature rely on point sources, as is typical for research tools. A production tool would most likely take the form of an evaporator with linear sources. As in the case of evaporation of copper indium gallium selenide

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(CIGS) materials, perovskite compositions suitable for tandem integration would require multiple chemical species being co-deposited with high spatial and chemical uniformity along with high deposition rates. This is not a trivial task, and it remains to be seen how toolmakers and research groups will respond to this challenge.

The other major classes of demonstrated scalable perovskite deposition methods are those based on slot-die coating. *Slot-die coating* is a well-established large-scale coating technology for several products in the semiconductor sector, including LCD display panels and xerographic photoreceptors. Several groups have reported in the literature high-efficiency single-junction devices with tandem suitable chemistries using this technique [39]. Moreover, the theoretical deposition time of a perovskite layer on an M6 wafer using this method is of the order of tens of seconds rather than tens of minutes. Additionally, these methods have already been demonstrated to be useful on tandems with chemically prepared surfaces [19,32].

Despite the demonstrated potential of the slot-die coating approach, significant challenges also exist. First, most examples in the literature rely on high-toxicity solvents such as N,N-dimethylformamide (DMF) for the perovskite ink. Large-scale production of PK/Si tandem solar cells would utilize large quantities of this solvent. Adequate controls to limit worker exposure and scrub this solvent from the factory exhaust could pose a significant challenge and incur additional processing cost. Other solvent systems do exist and in fact such a DMF-free solvent system was used in the example of a large-area blade-coated tandem shown in Fig. 1.

Another major challenge with slot-die coating of perovskite layers for PK/Si tandems is related to the geometry of the wafer itself. Unlike other applications where slot-die coating is deployed, a solar cell wafer uses its entire surface area to generate power. In a tandem application, this means that the perovskite top cell must be deposited as close to the edge of the wafer as possible for maximum efficiency. Moreover, the edge of the coating area must be as homogeneous as the rest of the coating area so as not to produce local areas of low efficiency.

A further challenge is the precise control over the beginning and ending of the coating zone. Slot-die coating often requires a small area at the start of the coating zone for the meniscus to equilibrate. Likewise, the end of the coating area requires careful control so that excess solvent is not left on the substrate. Finally, solar wafers are not perfectly square, which means that the effective coating width will change at different points along the coating path. As in the case of the co-evaporation process, solutions to these challenges will require significant support from toolmakers in the form of innovative tool design, tight process control and significant process optimization.

Apart from the two deposition examples described above, there are a number of other potentially scalable methods for perovskite deposition that could be utilized for large-area PK/Si tandems [40]. Some of these approaches, including ink-jet printing or spray coating, can produce single-junction laboratory solar cells with efficiencies approaching 20%. On paper, these deposition methods are extremely interesting and may be able to overcome some of the disadvantages of the two principal techniques covered here. However, these other methods have not yet been demonstrated on PK/Si tandem solar cells on any scale.

Back-end processes – metallization, interconnection and module fabrication

Following the deposition of the perovskite absorber layer and its contact materials onto a wafer, a tandem solar cell still requires several processing steps before a completed module can be obtained. These steps include screen-printed metallization, sorting, interconnection and finally encapsulation into the final module assembly. Because of the unique thermal and chemical compatibility of the perovskite solar cell, modification of these steps will be necessary, since the typical processing conditions used in commercial devices are not compatible with most current tandem devices. Undeterred by the fact that no completed modules have yet been demonstrated by the research community, several key advances have been made in the last few years which provide an insight into how these back-end processes could successfully be optimized for a PK/Si tandem solar cell.

Screen-printed deposition of a silver front grid is a standard process for practically all crystalline silicon solar cells. Modern processes allow very efficient Ag utilization to produce high-aspect-ratio silver fingers with good contact resistance and bulk conductivities to minimize spreading losses across the front electrode and across the device. For PK/Si tandem solar cells, nearly all laboratory cells utilize evaporated metal contacts, which can provide adequate current collection for small-area devices. However, full-wafer devices will most likely require a screen-printed Ag front grid for integration into existing solar cell process flows. The key challenge in achieving this is the low thermal budget available for curing the Ag ink after deposition. The group at CSEM has previously shown that this is indeed possible; however, the available silver pastes at the time resulted in a rather high contact resistance between the silver paste and the top transparent conductive oxide (TCO) of the tandem cell [41].

Since that initial publication, the availability of very low temperature silver pastes compatible with perovskite solar cells has increased dramatically. Internal tests within the laboratory at CSEM confirm that some of the best pastes are now able to achieve contact resistances of less than 10m$\Omega \cdot cm^2$ and bulk resistivities of less than $1 \times 10^{-5} \Omega \cdot cm$ while curing at

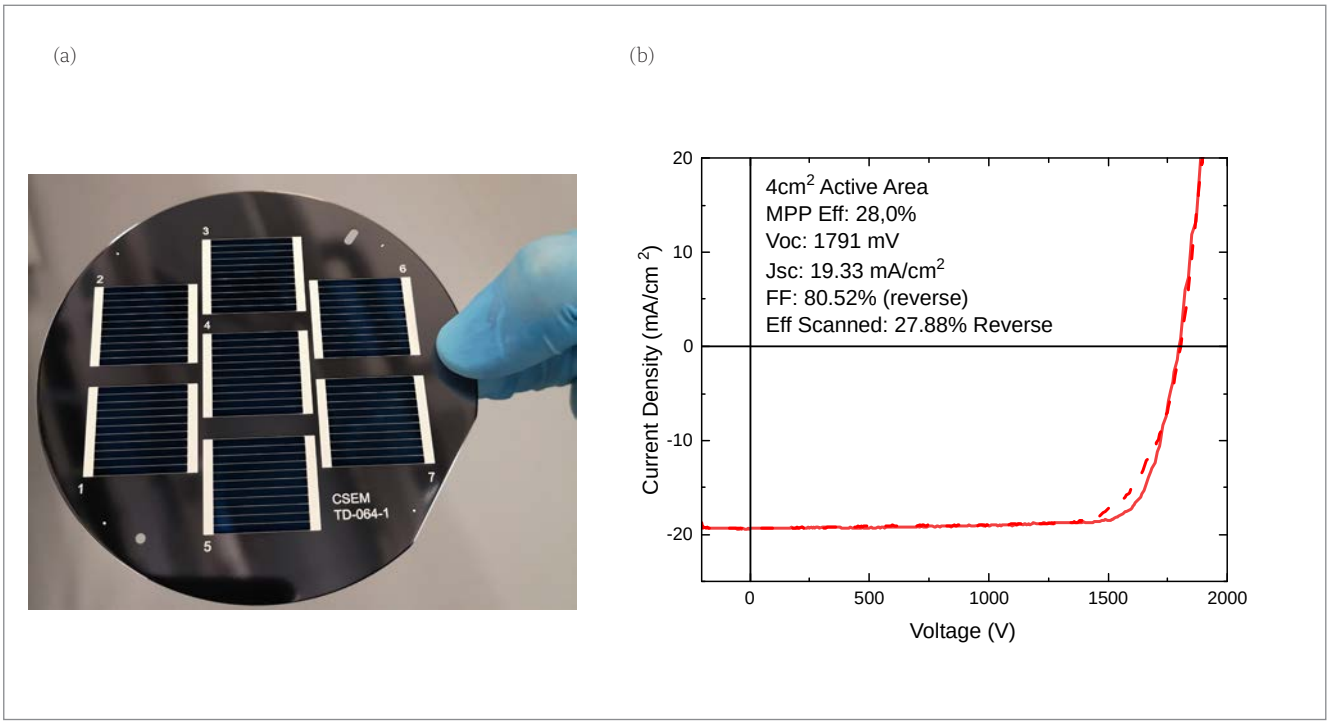

Figure 2. (a) A 4" FZ wafer with multiple PK/Si devices across its surface, including printed metallization. (b) LIV curve of a 4cm² PK/Si tandem with printed metallization, showing a fill factor of over 80% and a stabilized efficiency of 28.0%.

130°C. Such values now approach what is possible for silicon heterojunction solar cells.

These pastes are now being used routinely in the fabrication of the tandems in the group at CSEM (Fig. 2), where it has been possible to create cells with fill factors of more than 80% over a moderate area of 4cm² [23]. While the efficiencies of these devices are not currently on a par with those of the very best small-area cells, progress in this area shows that the front silver grid is not a barrier to achieving high-efficiency tandems over a large area. In addition, it would be remiss not to mention recent work demonstrating copper electroplating on perovskite devices [42]. This rather surprising work hints at the possibility of removing the Ag entirely from future tandem designs.

Similar to printed metallization, module assembly is another back-end process which requires careful consideration for use with PK/Si tandems. Because of the rather high sensitivity of perovskite devices to moisture ingress, PK/Si tandem modules would quite likely need to be assembled in a glass–glass configuration with a butyl edge seal. The actual encapsulation would take place during a lamination process, where pressure and temperature are applied to the stack to produce a hermetic seal. This process exposes the PK/Si tandem solar cell to potential thermal, mechanical and chemical degradation. A recent comprehensive review on the subject gives a far more detailed discussion of this [43].

Accounts can be found in the literature from a number of groups who have demonstrated processes to make encapsulated single-cell devices in order to test the stability of the cell to external stimuli [11,44]. However, in these previous examples the crucial encapsulant layer was omitted. Real-world cells require this encapsulant layer for improved mechanical strength of the module and for better optical coupling.

Very recently, several examples of glass–glass encapsulated PK/Si tandem solar cells with encapsulant layers were reported [45]. This idea was also demonstrated by the group at CSEM using somewhat larger cells with printed front metallization (Fig. 3). With careful optimization of encapsulant material and processing conditions, it was possible to achieve cell encapsulation with minimal degradation to the cell, except for a notable drop in the photocurrent of the cell due to the as yet unoptimized optics in the encapsulated stack. Otherwise, no obvious damage to the cell during the encapsulation processes was found. These preliminary results are very promising and show that a typical glass–glass encapsulation process can be successfully implemented in PK/Si tandem devices.

The glass–glass type of encapsulation scheme appears to provide sufficient isolation of the PK/Si cell from moisture ingress, as verified by damp-heat tests, where the best cells lost about 5% of their efficiency after 2,000h of stress testing. These initial results from the group at CSEM and

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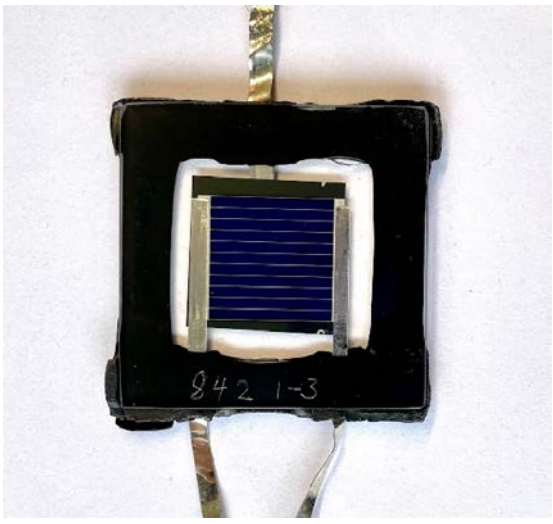
(a)



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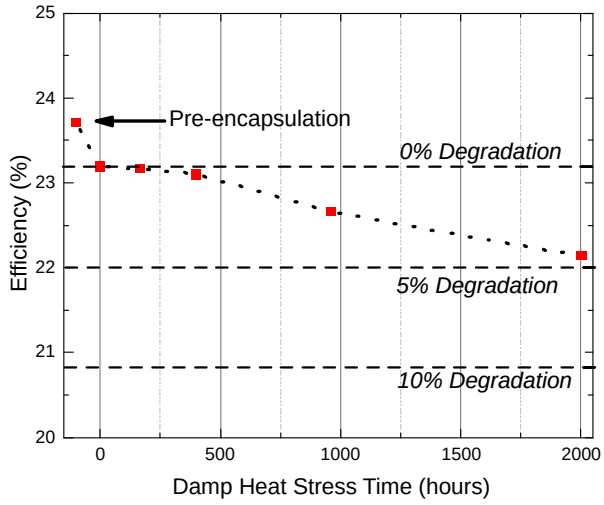

Figure 3. (a) Example of a 4cm² PK/Si tandem solar cell with printed metallization and glass–glass encapsulation with a butyl edge sealant. (b) Damp-heat stress testing of this cell, demonstrating approximately 5% degradation in efficiency after 2,000h at 85°C and 85% RH.

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others strongly suggest that modifications to standard glass–glass encapsulation processes could be a suitable starting point for the integration of PK/Si tandems into a standard PV process flow. Of course, further work on multiple cell interconnection for larger devices is still needed in order to investigate the various challenges that may exist here. In particular, the poor mechanical adhesion of some of the perovskite subcell layers may pose significant challenges in achieving reliable module-level interconnection [46].

One final area of note, which has received very little attention so far, is the measurement and sorting of PK/Si tandem devices prior to their module integration. This process is typically done to bin solar cells together in order to produce the best overall module performance. As is true for all industrial-scale processes, this measurement and sorting must be done extremely quickly (of the order of several hundred milliseconds per cell). Unfortunately, because of pseudo-capacitive effects and ionic movement within the perovskite solar, the high speeds can greatly distort the cell performance measurements [47]. Future work to look into this issue will be another necessary step on the road to integrating PK/Si tandem solar cells into existing process flows.

Conclusions and outlook

In summary, the development of two-terminal PK/Si tandems continues to advance at a respectable rate. The steady rise in record cell efficiency is seeing the emergence of a diverse collection of processing pathways towards building efficient tandem devices. For the most part, these different processing pathways are the result of research groups identifying and finding unique solutions to the many challenges faced in terms of materials and processing. These advances have touched on every aspect of the solar cell process flow, from wafer texturing to module encapsulation. Indeed, it is encouraging that many researchers are actively focusing on meeting the challenges of scale-up rather than simply looking to improve device efficiency.

These excellent advances, however, have not yet translated to the engineering of large-area devices which incorporate many features of standard solar cell devices (such as commercial CZ wafers, large-scale PK deposition and printed metallization). This is hardly a criticism of the field, as such work can demand significant resources and access to certain toolsets. Recent investments in this area by a number of established PV manufacturers will probably change this state of affairs in the near future. Regardless, major challenges still exist in finding a deposition process for the perovskite layer that is both high throughput and forms a high-quality material. Additionally, many open research questions exist in respect of the module lay-up process of these types of solar cell and how their unique physical properties will affect module reliability and stability.

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