When heterojunction meets shingle: R&D activities at CEA-INES

Samuel Harrison[1], Carolyn Carriere[1], Vincent Barth[1], Armand Bettinelli[1], Baptiste Portaluppi[1], Valentin Giglia[1] & Marco Galiazzo[2]

[1]Grenoble Alpes University, CEA-LITEN, DTS, INES, Grenoble, France; [2]Applied Materials Italia Srl, Baccini Cell Systems, Treviso, Italy

Abstract

The recent announcements along with the latest very high-power modules reported by the various leading manufacturers clearly indicate that the requirements for module production are rapidly shifting towards new standards, where many new concepts are beginning to emerge. Among these techniques, 'zero-gap', paving and shingling integration in particular are attracting a lot of attention, as they can combine very high efficiencies with improved aesthetics, which are necessary for many PV applications, such as rooftop integration or more general building-integrated PV (BIPV) and vehicle-integrated PV (VIPV). In addition to this denser integration scheme, the incorporation of a 'cut cell' is becoming the norm, because with the increase in both cell efficiency and wafer size (the shift from M2 to M6 and even to M12), it is essential to limit the resistive losses linked to the very high currents generated by such devices. Commercial modules in such configurations are already available, but these are mostly built with technology based on the passivated emitter and rear cell (PERC) concept. Indeed, high open-circuit voltage (V_{oc}) cell configurations, and especially heterojunction (SHJ) architectures, may not appear at first sight to be the most suited to shingling, as performance losses can be fairly significant with the unpassivated edges generated during the cutting step. But, on the other hand, SHJ technology already benefits naturally from the extensive know-how acquired when combining electrically conductive adhesive (ECA) with transparent conductive oxide (TCO) and low-temperature metal pastes. Furthermore, the cell-to-cell overlap significantly decreases the impact of cut-edge defects, thereby minimizing the effective efficiency losses. This paper will accordingly outline the recent activities at CEA-INES concerning the development and understanding of the integration of such shingle cells. The initial focus will be on the impact of the cutting step on final cell characteristics, highlighting the outcomes and challenges related to this critical process step. The main achievements in interconnection and module integration will then be described, with specifically the fabrication of ~400W solar panels featuring high reliability.

Introduction

On the one hand, there is the silicon heterojunction (SHJ) device, which is one of the most attractive technologies, combining high power and a simple fabrication process flow (Fig. 1(a)). Efficiencies greater than 25% on large-area devices have been demonstrated by several companies/institutes [1–3], including recent announcements from CEA-INES [4], proving that the transfer from lab-scale to high production volume is currently accelerating. However, SHJ has also recently faced new challenges, as the module integration scheme is progressively moving towards half-cell or even shingle interconnection. Indeed, as presented in previous publications [5,6], noticeably severe performance losses are observed when SHJ cells are cut, linked to the creation of an unpassivated edge. Several investigative studies on cut optimization or edge repassivation have been conducted, but, so far, most institutes/companies have reported final cell efficiencies lower than the initial full-cell performances [7,8].

"Noticeably severe performance losses are observed when SHJ cells are cut, linked to the creation of an unpassivated edge."

On the other hand, there is the shingle interconnection scheme, which is quite an old concept (first patented in 1956 – see Fig. 1(b)), but currently regaining more and more interest, as it combines several advantages and appears to be particularly adaptable to new PV challenges. In fact, with the increased active area linked to the tile overlap, and the low electrical resistance of the assembled interconnection, very high-power densities are achievable [9]. Furthermore, because of the formed uninterrupted silicon array, and the absence of interconnection wires or ribbons, the global aesthetics are significantly improved, thus meeting the new demands and requirements for large-scale deployment in building and vehicle applications.

But what happens when SHJ and shingle concepts are combined? Certainly, the consequences of moving towards this new module design must be properly evaluated, not only in terms of module final performance but also in terms of long-term module stability and reliability. Such analysis has already been initiated by Gérenton et al. [10] for half-cell configurations, but even stricter constraints can become apparent when a shingle interconnection is considered. As shown in Harrison et al. [6], up to $1\%_{abs}$ efficiency losses can be observed after cutting an SHJ cell in a thin shingle stripe configuration. These losses, however, are expected to be reduced after module integration, since no carriers will be generated next to one of the defective edges thanks to the shading created by the natural cell overlap that occurs in shingle integration. Furthermore, the need for ECA in shingle interconnection seems particularly well suited to an SHJ configuration, as the interactions of this type of conductive paste with ITO and low-temperature paste have already

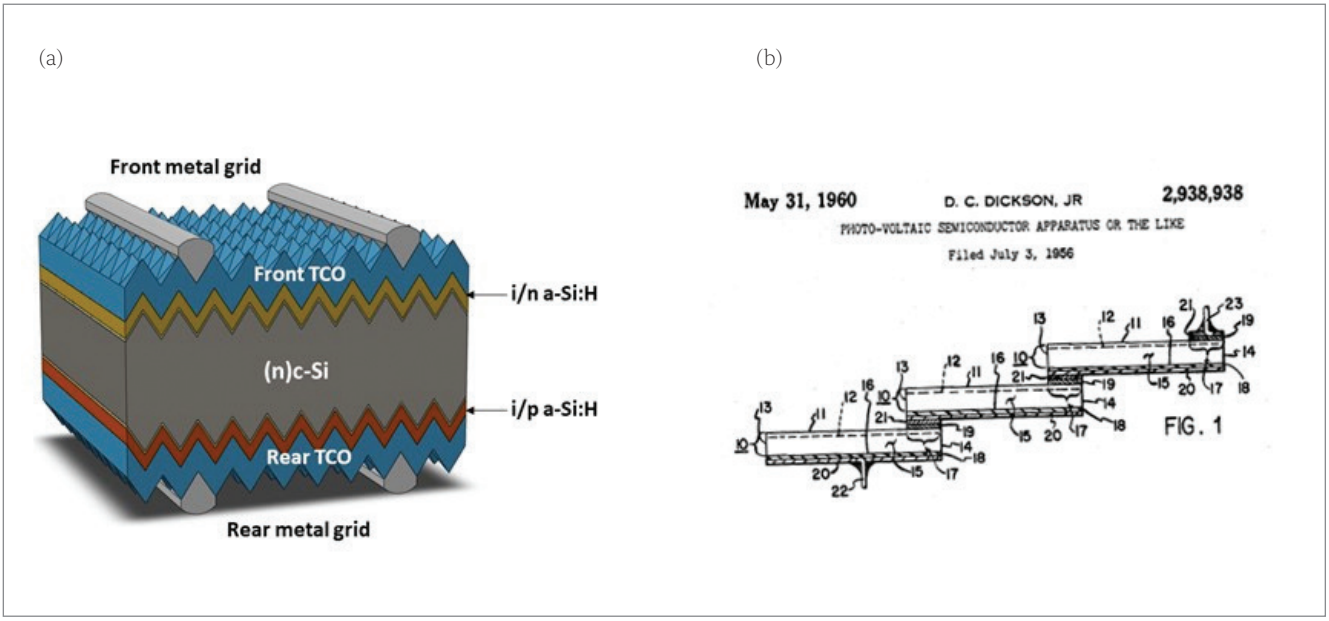


Figure 1. (a) Schematic of the heterojunction cell device used. (b) Picture taken from a 1960 patent, already describing the shingle concept in use today.

been widely studied, especially for traditional ribbon attachment [11].

This paper will first introduce the specific constraints and achievements with regard to the SHJ shingle cell, before presenting the development work conducted using the CEA-INES production line. Finally, major interconnection and module results will be detailed, with in particular the fabrication of the first large-area device (equivalent to 72 cells), for which promising power and reliability results have already been demonstrated.

Shingle SHJ cells

The core process of the SHJ shingle cells remains unchanged, meaning that all texturization, cleaning and deposition steps are identical to standard production processes [12]. However, if the metallization step still relies on screen-printing for the paste transfer, it will need to be adjusted to the specific shingle configuration. Indeed, for shingle cells, the busbar is relegated to the edge of each tile; while this imposes an interrupted finger design, as described in Fig. 2, it also leads to very effective longer metal lines, twice the length they would otherwise be in a conventional centred six-busbar design.

As the metal paste conductivity is limited by the heterojunction temperature constraints, a double-print process is introduced for the front side [13], allowing a good compromise to be achieved between overall finger optical shading and high cell performance. On the back side, in contrast, a simple print process is retained, as the dense grid pattern used for standard cells is sufficient for limiting the parasitic resistance. The paste consumption increase, when compared with standard SHJ devices, remains thus limited, even

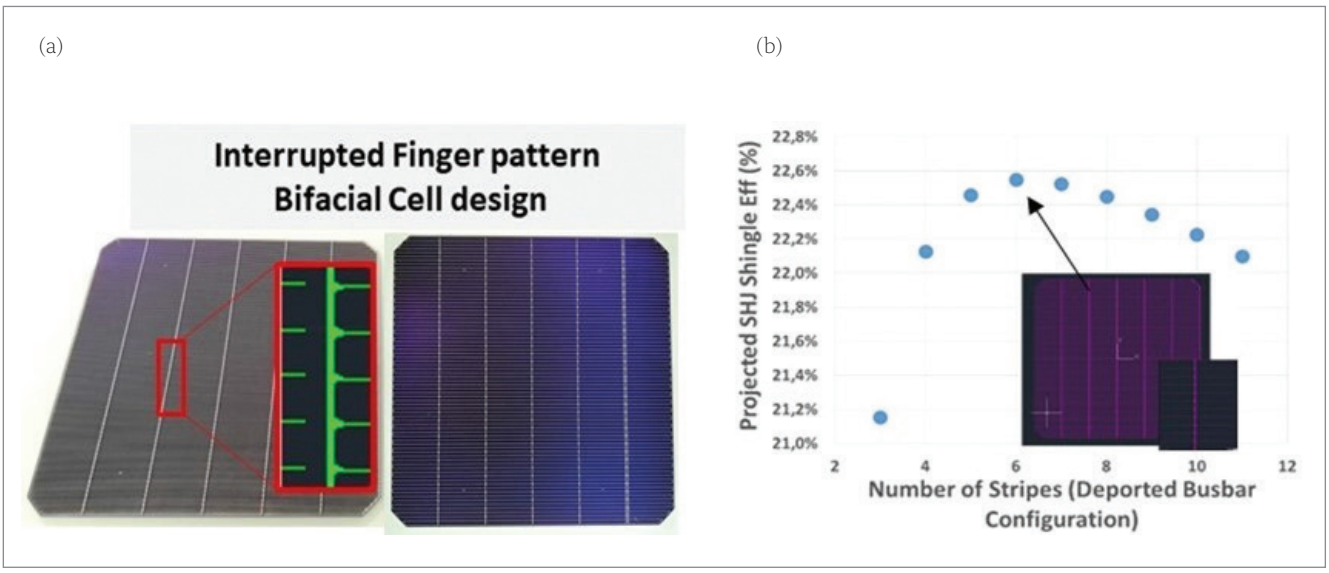


Figure 2. (a) Photo of a fabricated SHJ shingle cell, with a schematic of the specific busbar and interrupted finger design. (b) Optimization of SHJ shingle tile length, to reach a compromise between metal resistance and cut-edge impact.

Figure 3. CEA-INES heterojunction production line. All the shingle cells were manufactured on this industrial platform.

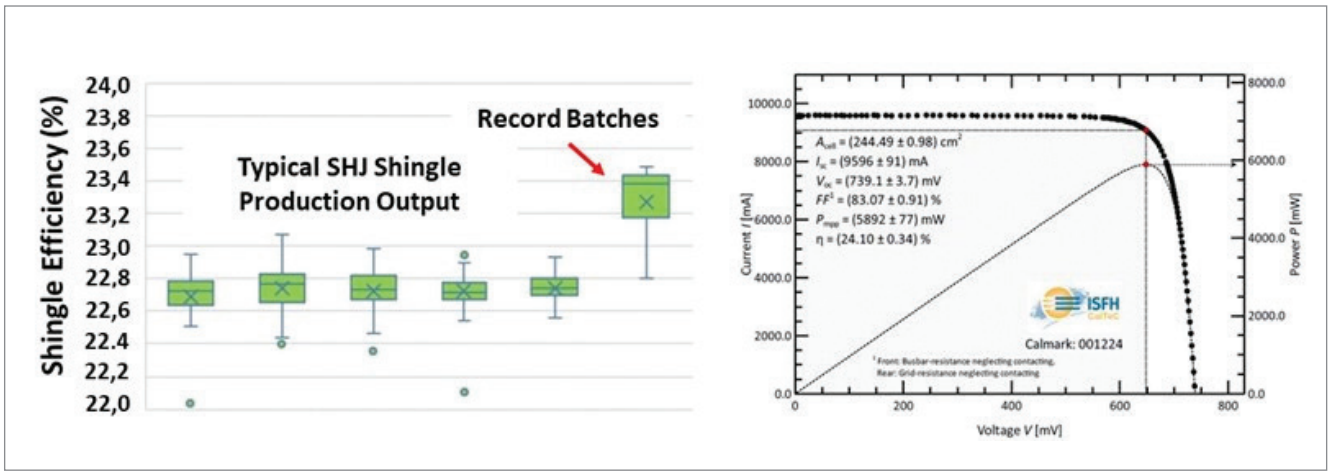


Figure 4. (a) Typical efficiencies obtained with SHJ shingle cells on the CEA-INES production line. (b) Record shingle cell certified @ 24.1%.

"A six-stripe configuration (26mm tile length, M2 size wafers) appears to be the optimum choice for a satisfactory compromise between cut-edge impact and global metal resistance."

if further developments or alternative metallization schemes [14,15] might be beneficial to improve the competitiveness of such cells.

Small length tiles could therefore be interesting for SHJ, but to define the optimum tile length, it is also necessary to take into account the losses in efficiency after the cut. As will be described in the next section, the performance can be significantly degraded if tile dimensions that are too small are considered. Finally, a six-stripe configuration (26mm tile length, M2 size wafers) appears to be the optimum choice for a satisfactory compromise between cut-edge impact and global metal resistance. Such a tile length is still fully compatible with industrial constraints, and suitable with regard to current stringer constraints. Finally, it is worth noting that the shingle cell design remains highly bifacial (>85%), and can still benefit from the power increase linked to illumination albedo, with this being taking into account, if possible, during the system installation.

Solar cell batches – compatibility with high-efficiency requirements

Shingle cells used in this study were all produced on the CEA-INES industrial 'LabFab' platform (Fig. 3), as described in the previous section. Thousands of cells (>4,000 cells) were fabricated, with typical average efficiencies measured in the 22.6–22.8% range (Fig. 4(a)), illustrating the perfect compatibility of the adapted process to a standard production line. It is worth mentioning that, with simple process improvements and diminished throughput, record batches with up to 23.4% efficiencies were obtained, demonstrating the possibility of achieving very high efficiencies with this technology. The record cell was certified at 24.1% (full M2 size), although the production process included an additional technological step that was not fully compatible with current high-throughput constraints (Fig. 4(b)). This excellent result demonstrates, however, that there is potential margin for optimization, and that the SHJ shingle configuration is fully consistent with high-performance needs.

Cutting step impact

Cutting is the most critical process step for shingle heterojunction devices. Indeed, the high bulk quality, coupled with the absence of a strong internal field effect and the very high passivation levels reached for the SHJ architecture, leads to very high sensitivity of the structure to the edge defects generated during the cutting step [16,17]. Simulation studies even show that the edge defect impact can extend up to 3mm inside the bulk, thus greatly affecting the charge recombination and the final fill factor (*FF*) achievable [18]. In a half-cell configuration, up to

0.3%$_{abs}$ efficiency losses are generally measured after separation. For shingle tiles, the situation is even worse: because of the lower surface to perimeter ratio, and the creation of two defective edges, up to 1%$_{abs}$ losses can be observed on the final devices (Fig. 5).

Such a high level of edge defectiveness is thus clearly a critical limiting factor, and many development studies have been initiated in order to optimize and better understand how to limit the associated performance losses. For heterojunction devices, it is mandatory to limit as much as possible the parasitic heating that occurs during the separation process; for traditional laser-cutting approaches, this translates into only partial silicon ablation (typically, it is necessary to target a scribe length of one-third of the initial wafer thickness), followed by mechanical breakage. Several laser passes are considered for the ablation step to limit the heating. Despite the precautions taken, however, both active layers and silicon bulk volume show fairly significant morphology degradation around the newly created open edge [8]. Consequently, alternative cutting techniques have also been evaluated. It is worth mentioning in particular the thermal laser separation (TLS) approach [19,20], developed by the company 3DMicromac, as well as an innovative integration proposed by CEA and relying on 45°-rotated ingots [21]. The TLS concept relies essentially on thermal mismatch for the crack propagation, while the 45° ingot concept takes advantage of the natural privileged (110) crystalline fracture line that is thus now aligned with the desired cut lines, allowing a full mechanical separation process.

Nevertheless, as shown in Fig. 6, the final efficiency losses all remain very similar, measured again in the 0.25–0.3%$_{abs}$ loss range. This highlights that if the cutting process (in particular the laser-based scribing) is properly optimized, the damage inflicted upon the SHJ device remains limited, and the main losses observed are essentially linked to the extremely high impact of the generated unpassivated edges. This finding is particularly true for SHJ architectures, again because of the very high carrier lifetimes observed in such devices, but will probably apply to all alternative architectures, such as tunnel oxide passivated contact (TopCON) or poly-Si-based structures, whose passivation levels are also reaching very high levels.

A comparison of the three cutting techniques shows clearly very different cut-edge morphologies, with very smooth surfaces obtained for both the TLS and the 45° ingot approaches. This morphological improvement is essential for two major reasons. First, the likely reduction in local micro-cracks will help to lower the overall breakage rate when module production is considered. Second, as mentioned previously, edge repassivation might be mandatory in order to mitigate the observed losses and recover performance; all research activities published so far, however, show that such processes are not compatible with laser-based scribing methods [6,7,22].

Cut-edge defectiveness: how to moderate its impact?

It would not be appropriate to go into too much detail in this overview, as much R&D activity is currently still ongoing, and the current assumptions and findings may rapidly change over the

"The main losses observed are essentially linked to the extremely high impact of the generated unpassivated edges."

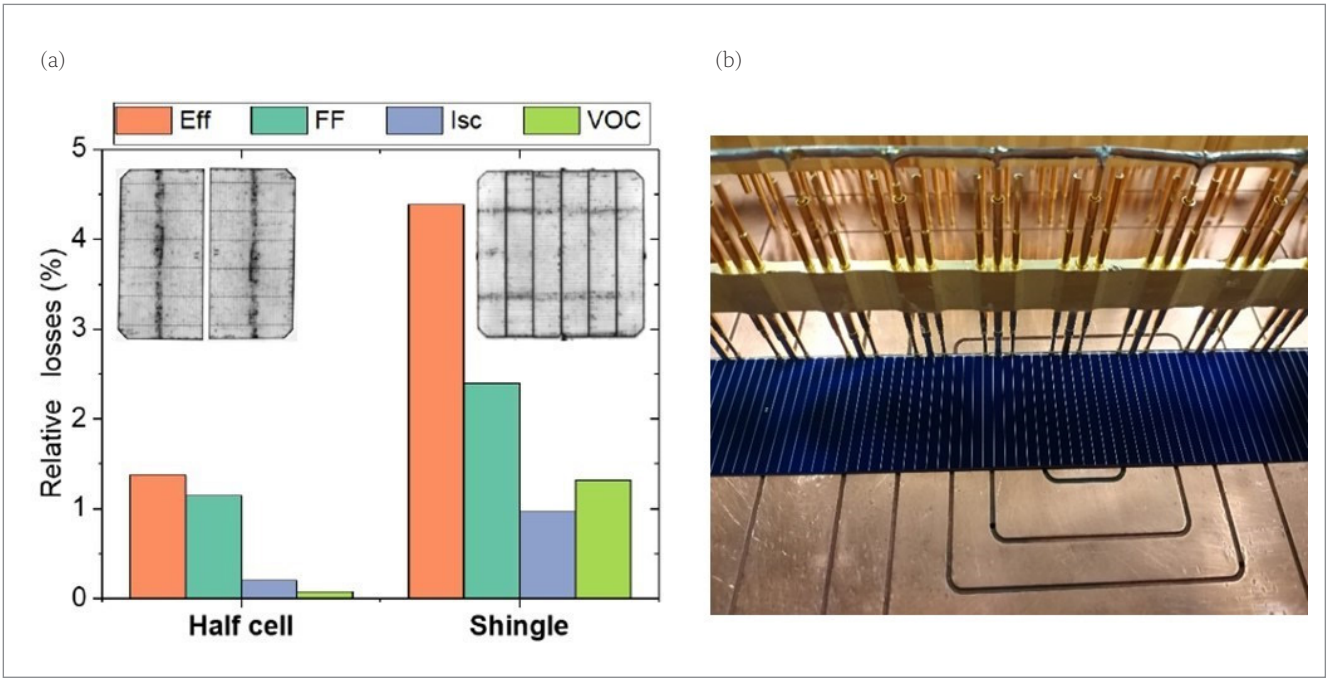


Figure 5. (a) Typical efficiency losses measured after cell separation for half-cell and shingle configurations. (b) The measurement set-up for an isolated shingle tile.

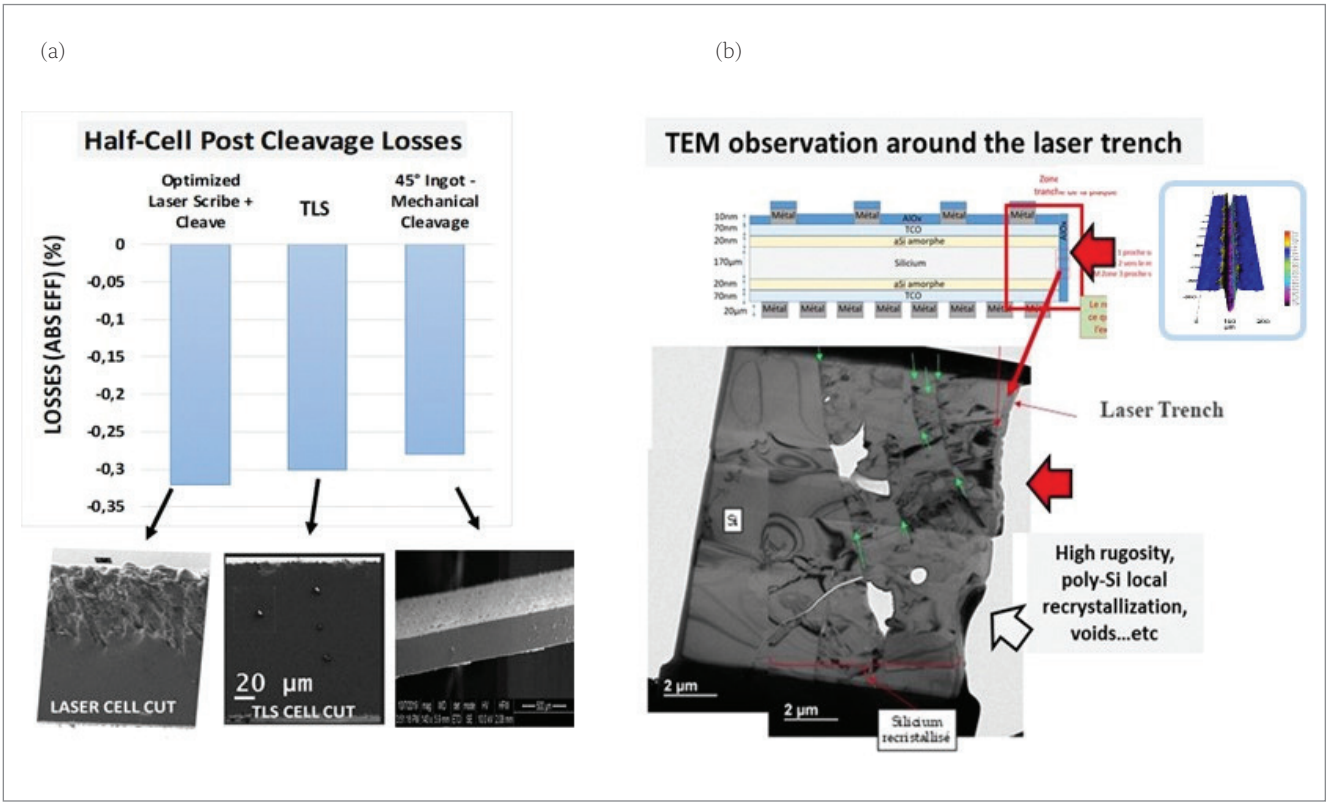


Figure 6. (a) Comparison of different cutting techniques. If very similar performance losses are observed, the final cut-edge morphology shows a smooth appearance for the TLS and 45° ingot approaches. (b) Strong degradation of both active layers and silicon bulk around the laser trench is confirmed by local transmission electron microscopy (TEM) observations.

coming months with the expected technological improvements and the rapid emergence of innovative solutions. However, it would be useful to mention several activities that could lead, either separately or cumulatively, to a significant reduction in the observed apparent losses due to cutting.

First, it is worth pointing out that, because of the specific shingle configuration, a natural cell-to-cell overlap occurs, meaning that one of the defective edges is shadowed by the adjacent integrated tile. This is important, since free carriers are therefore generated further away from the cut-edge, thus minimizing its true impact when integrated in the final module. This is illustrated by the *I–V* measurements shown in Fig. 7, in which an *FF* gain, for example, can be clearly seen when the masked edge length is progressively increased. However, this cell-to-cell overlap increase must remain limited when the final product is considered, as a compromise between performance

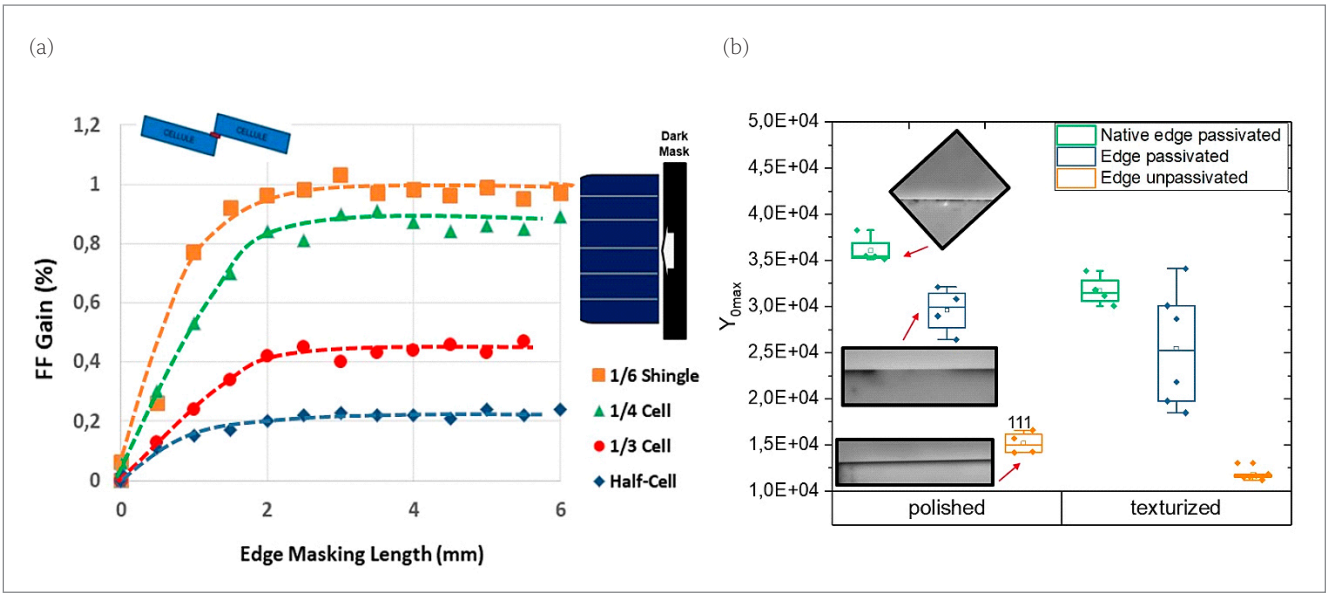


Figure 7. Illustration of paths of improvement for minimizing the impact of edge defectiveness. (a) Improvement that happens naturally, thanks to the cell-to-cell overlap. Significant performance recovery can be realized with a moderate overlap of, for example, 1mm. (b) Additional process steps, dedicated to edge passivation might be necessary to further improve the module power. This graph shows that the local deposition of amorphous silicon allows a distinct recovery of lost performance (Y_0 metric based on PL edge signal extraction; high values of Y_0 represents high passivation values).

Figure 8. BSC SONETTO stringer developed by Amat-Baccini, with additional images of the strings produced, as well as of the typical stripes obtained after the cutting of the cell.

recovery, final product power and overall cost might need to be found.

With regard to the edge passivation approach, many ideas are being tested [7,8,23,24], but no clear technological solution has emerged yet. The topic is indeed quite complex for SHJ, mainly because of the temperature constraints; the importance of hydrogenation and the need for very clean and smooth edge morphology both appear to be critical in order to reach locally the necessary high passivation levels to improve the performance of the cut cell. However, the initial results obtained, mostly with the deposition of appropriate layers on the cell edge (amorphous silicon, AlO_x or SiN_x, for example), demonstrate that promising improvement paths are certainly possible, even if only partial recovery has so far been achieved in internal investigations [6,25].

Alternative optimization paths (not mentioned in this article) can also be considered, with in situ passivation during the cutting step, the use of organics or polymers for the edge passivation, and an optimization of the cell integration process (for example, the use of low-resistivity wafers, or an optimization of TCO edge exclusion). In all cases, the implications of additional dedicated passivation steps must be properly assessed at the industrialization level, and the impact on both integration complexity and overall product cost needs to be evaluated in some detail.

Interconnection

A completely new interconnection scheme had to be developed for SHJ shingle purposes. ECA is already widely used for conventional ribbon-gluing interconnection, which is one of the most common interconnection approaches developed for standard SHJ modules. Thanks to the extensive know-how acquired when combining ECA with both metal paste and TCO, it was possible to define an adequate metal pattern for shingling in the interconnection area; the cell-to-cell adhesion is optimized, with sufficient contact area between ITO and ECA, while ensuring proper electrical continuity between the metal lines/busbar in contact with the ECA [26]. To limit the ECA consumption, regular pads of ECA are deposited instead of continuous paste deposition.

Interconnection development and string realization were a joint undertaking with the company Amat-Baccini, located near Treviso in Italy. All strings were fabricated on its dedicated BSC SONETTO industrial equipment (Fig. 8), which allows in succession:

1. Cell scribing and mechanical cleaving.
2. Deposition of the ECA on the Ag pads present on the busbars.
3. Alignment of the cut cells, or shingles, to form the string.
4. Attachment of the end ribbons to the string via ECA.
5. Final curing process.

The fully automated equipment adopted for the test is based on:

- A laser platform with a galvanometer scanner.
- A screen-printing system to deposit the ECA, with a typical printing speed of 200–300mm/s.
- Linear motion units to handle the shingles with precision.
- An integrated device to deposit and align the end ribbons to the string.
- A continuous oven capable of performing the curing with a maximum process window of 200°C and 90 seconds.

The equipment was tested at 4,000 wph in a dual-lane configuration.

It was then possible to rapidly assemble several small-dimension strings to validate the different technical choices made, and to optimize the overall process. This preliminary work allowed in particular to confirm the good compatibility of the ECA chosen with the metal design specifics, to optimize the

"A completely new interconnection scheme had to be developed for SHJ shingle purposes."

integration conditions (pressure, curing temperatures, etc.), and to build the first mini-module. This mini-module was submitted without delay to the usual ageing tests (thermal cycling – TC – in particular, which is the most critical for the shingle configuration). The TC tests revealed excellent reliability, with power losses less than 2% observed after up to 800 TC cycles (Fig. 9); this is an excellent result, confirming the perfect match between SHJ architecture and shingle interconnection [27].

Further experiments were subsequently conducted to further optimize the stringing. It was possible to validate that the developed process remains fully reliable with a significant reduction in ECA consumption, dropping from ~20mg to ~12mg per cell (only 2mg per tile!), which represents almost a 50% material saving without power or reliability degradation.

Similarly, it was proposed to evaluate whether using thinner wafers, down to a thickness of 120µm (which is expected to soon become the norm), could affect the defined interconnection scheme. Again, very good output power values were achieved at the mini-module level (equivalent to a two-cell configuration), with excellent reliability. The breakage rate remained unchanged, despite the thinner material used, and very limited process modifications were necessary – essentially during the final curing step to avoid excessive bowing of the wafers.

Examples, and details of the interconnection trials performed, are presented in Fig. 10, along with microscopic images of the interconnection pads and the ECA used. Following these promising initial sets of results, upscaling of the technology was initiated and the first large-area modules built, as described in the next section. It is worth noting that, even if the process developed is already very satisfactory, a margin for optimization may still be possible. Development work is currently under way to reduce the cell-to-cell overlap down to 0.5mm, or to increase the global throughput of the stringer tool, which could soon demonstrate that even better results might be achieved with SHJ shingle technology.

Upscaling and large-size module integration

The promising results obtained for a mini-module configuration now needed to be successfully transferred to a long-string configuration. A 37-tile configuration was first chosen (string ~1m in length), with a cell-to-cell overlap of 1mm. This length of overlap appears to be a good compromise between active area silicon integration and ease of fabrication, as it allows a comfortable margin in the successive critical alignment steps needed for a proper shingle integration: 1) front and back metallization; 2) ECA with metallization; 3) laser cutting; 4) cell-to-cell automated placement. Furthermore, as illustrated in Fig. 7, it may not be so interesting to switch to more aggressive overlaps, since part of the power gain could be masked by the greater impact of the defective edge. However, experiments to study the impact of a tighter overlap (down to 0.5mm overlap) are already in progress, and preliminary results should be soon available.

"The TC tests revealed excellent reliability, with power losses less than 2% observed after up to 800 TC cycles."

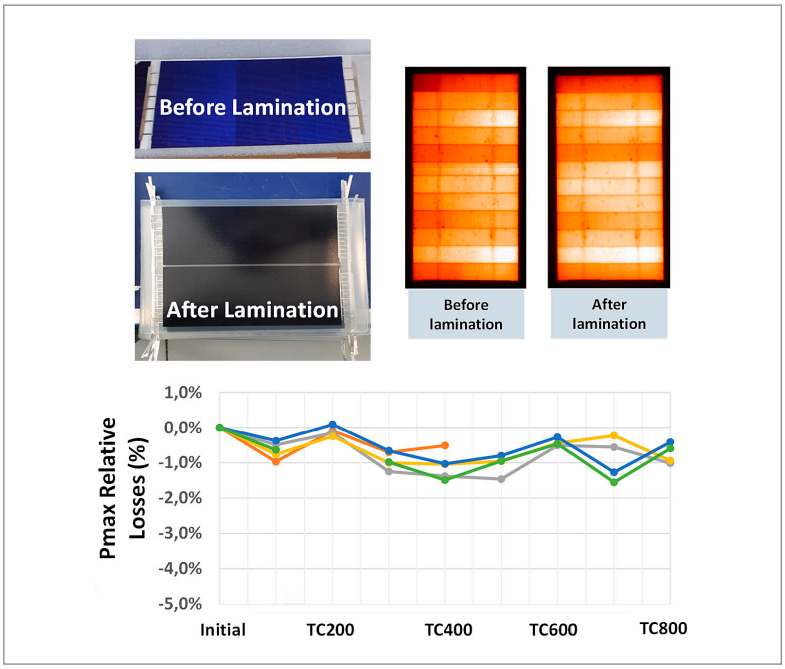


Figure 9. Example of SHJ technology development undertaken at the mini-module level. Outstanding reliability was obtained, and no evidence of cell breakage or degradation was observed during the lamination step.

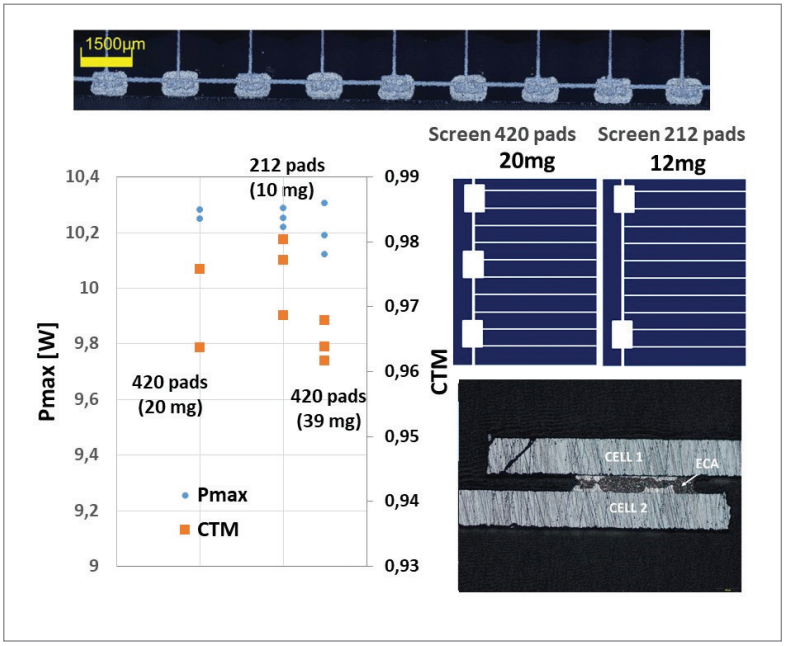


Figure 10. One of the most promising paths of interconnection improvement is the possible reduction of ECA paste consumption. The top image shows a perfect alignment of the ECA with the metal pads used, and the total amount of ECA deposited can easily be reduced either during the printing step or by using a fewer number of metal pads. Excellent power and cell-to-module (CTM) ratio results are obtained (bottom images), even with a minimal usage of ECA (12mg for six tiles, equating to just 2mg per tile). The reliability also remains excellent (not shown here).

Despite only 200 TC having been completed at the time of writing, the initial ageing tests conducted on this intermediate module configuration seem to confirm the excellent reliability of the technology, and the greater dimensions of the manufactured strings do not translate to increased fragility during manipulation or lamination [27]. As shown in Fig. 11, very similar output power and reliability results are again observed with thinner wafers (120µm thick), and the behaviour seen is very close to that of a mature alternative interconnection scheme, such as SmartWire Connection Technology (SWCT).

"Excellent module outputs were achieved, with up to 396W being measured on the module with a semitransparent backsheet."

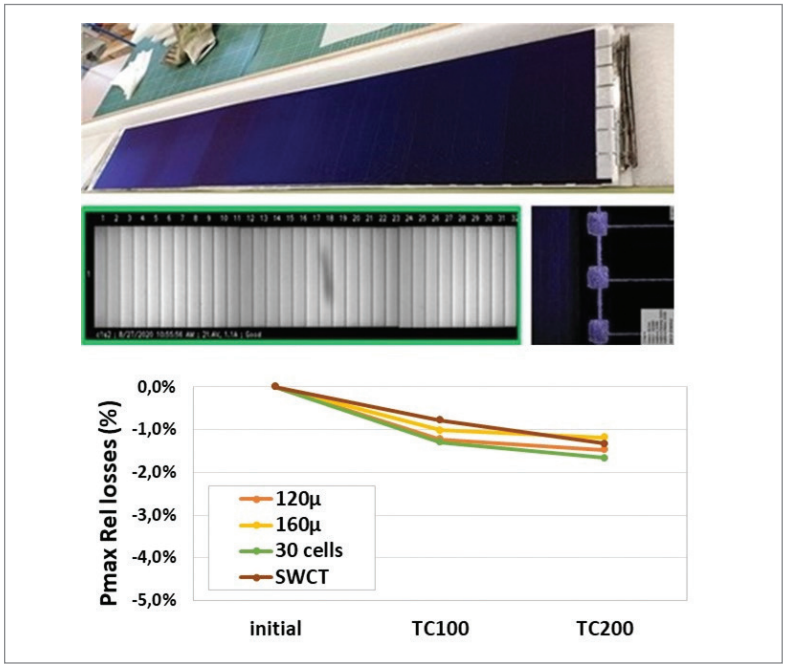


Figure 11. Successful upscaling of SHJ shingle technology. Shingle strings ~1m long were successfully assembled, yielding excellent initial reliability results (200 TC cycles achieved so far).

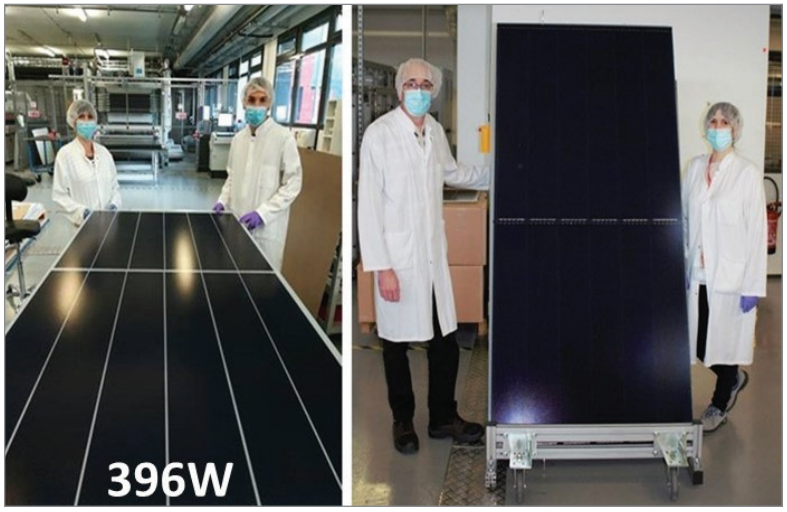


Figure 12. The two fabricated large-area SHJ shingle modules. Close to 400W was measured for the best module, demonstrating the high potential of SHJ shingle technology.

Finally, the first large-area modules were fabricated (Fig. 12) with the interconnection scheme that had been extensively validated by the smaller module configuration [28]. In particular, a cell-to-cell overlap of 1mm was kept, and a total ECA amount of 20mg per cell (six shingle tiles) deposited. Cells with an average efficiency of 22.7% (average production output) were integrated. Further experiments using record batches (average efficiencies of up to 23.4%), however, will be initiated soon, as a higher volume of production is still necessary for large-module considerations.

A standard glass dimension of 2,029×998mm² (equivalent to 72 cells, standard glass) was chosen, even though with this size, the filling of the module with the shingle tiles is still not optimum. The modules were assembled with 12 vertical strings, each integrating 39 SHJ shingle tiles. The first module was integrated with a semitransparent backsheet (85% transparency), with a focus on module performance, reliability and bifaciality. The second module was integrated with a black backsheet, where not only power but also global aesthetics are the priority.

Excellent module outputs were achieved, with up to 396W being measured on the module with a semitransparent backsheet. A module efficiency of 21.6% was calculated when just the active area was considered, as the glass size used was not perfectly adapted to the string length produced. However, with a CTM ratio of 94% (including the cell-cutting losses), and a global bifaciality ratio of 86%, the high potential of combining SHJ and shingle has already been demonstrated. (Although 86% is a satisfactory, considering the semitransparent backsheet, this value will be improved with the use of a glass–glass module configuration). A significant increase in module power output is nevertheless still expected, thanks to a combination of higher cell efficiencies and further optimizations of module integration.

Module optimization: what's next?

Many optimization paths can still be explored for the developed SHJ shingle technology, and even more competitive module powers and costs are probably achievable with limited process adjustment. The edge passivation trials have already been mentioned, but there is also a potential margin for optimization in the metal-interconnection scheme itself.

The simulation tool CTMOD, developed at CEA [29], was used to further examine if an alternative cell metallization compromise was possible, and if a better compromise between silver consumption and performance could be defined. The simulations carried out for a 78-cell-equivalent shingle module (M2 cells cut into six pieces) show, for instance, the impact of the front and the rear metal grid pitch. Finger width is fixed at 70µm, as measured experimentally on standard shingle cells. Regarding the front grid, the optimum pitch was found to be around 1.8mm, even though module performance does not vary very much in the 1.5 to 2.1mm pitch

range (ΔP_{max} < 1.5W). In contrast, modification of the rear grid pitch has a tremendous impact: reducing the pitch from 0.7mm to 0.35mm, for example, allows a power increase of about 5W, but at the cost of double the total silver consumption for the back side (Fig. 13).

Another important topic is the optimization of the cell-to-cell overlap. As mentioned previously, a conservative overlap of 1mm was retained for the shingle experiments presented in this paper. However, moving towards a 0.5mm overlap would allow an important gain in power (almost 10W for a 72-cell-equivalent module, equating to a 2% power increase). But, at the same time, because of this smaller overlap, each constructed string would end up being longer (~19mm longer strings for the 72-cell-equivalent module considered). The longer string dimension would require an increased module size, ultimately leading to a reduction in the final efficiency obtained for such a module configuration (Fig. 14). There are thus different possible compromises possible when the final module configuration is defined, depending on the main driver that needs to be maximized (P_{mpp} or efficiency) for the module application.

Finally, the upscaling of the technology towards long strings or large-area modules was already discussed in the previous section, but what about the upscaling of the wafer size, which is happening today in the PV market? The number of stripes per cell is undoubtedly a compromise between edge-cutting losses and resistive losses linked to the cell metallization. By moving to M12 wafer size, the fact that more cuts are necessary to achieve an optimum module power becomes all the more obvious. The CTMOD simulations did indeed predict that for an M12 cell module, each cell should be cut into seven pieces, for a final width of~30mm for each sub-cell (Fig. 15). If this would be beneficial in decreasing the relative impact of the edge-losses, solutions to improve the metal line resistance would nevertheless still be required.

Conclusion and perspectives

This paper has provided an overview of the different opportunities, but also the challenges, associated with the integration of SHJ technology in a shingle configuration. Indeed, despite many shingle modules being already commercially available, to the authors' knowledge they mostly integrate standard technology, such as PERC devices. Although SHJ technology is naturally well suited to the shingle interconnection, with excellent results having been obtained at both the cell and the module level, optimization is still necessary in order to take full advantage of the very high efficiencies brought about by the use of SHJ.

The performance loss after the cutting step remains high, but several technical solutions for loss recovery are currently under development at the laboratory level. Similarly, metal paste consumption is higher because of the greater length of the metal lines due to the relegated busbar configuration. An alternative metallization solution might need to be considered (for example plating), even if the impact on final cell cost of ownership (CoO) remains limited (Fig. 16). Nevertheless, with a record cell certified at 24.1%, and modules fabricated with power values close to 400W, the high potential of SHJ shingle technology has been demonstrated. With further

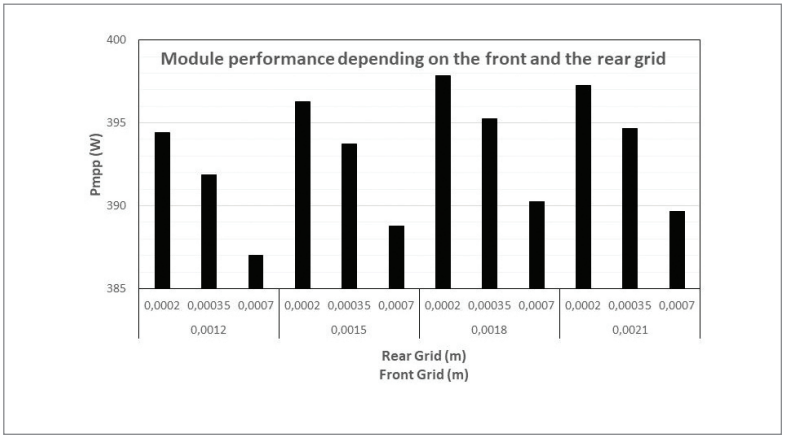


Figure 13. Simulated impact of the front and back cell metal pitch on final SHJ module output power. As shown, a greater margin for optimization (compromise between silver consumption – cost – and module power) can be achieved with a reduction of the back-side metal pitch.

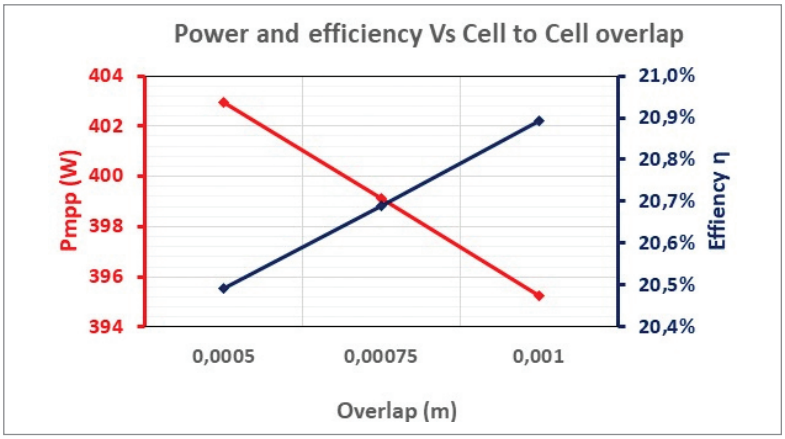


Figure 14. Simulated SHJ shingle module power and efficiency for different cell-to-cell overlaps. Higher power can be obtained with a smaller overlap, but because of the increased final string length, the module dimension needs to be adjusted, ultimately resulting in lower module efficiencies.

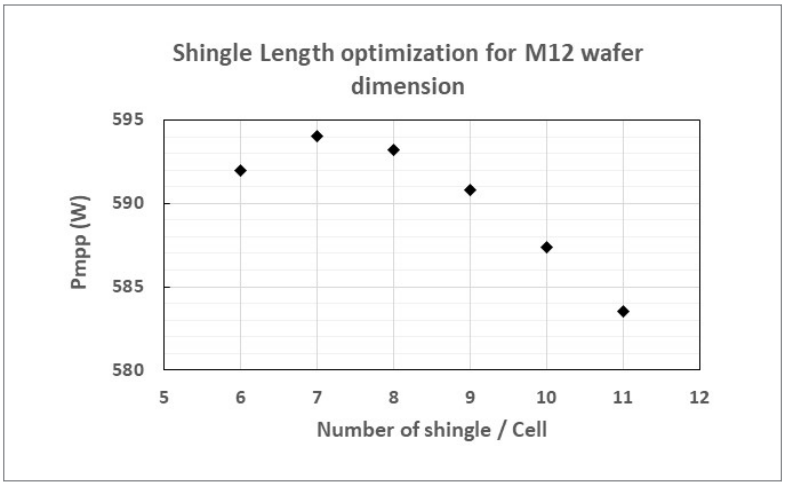


Figure 15. Optimization of SHJ shingle width for M12 wafer size.

"With a record cell certified at 24.1%, and modules fabricated with power values close to 400W, the high potential of SHJ shingle technology has been demonstrated."

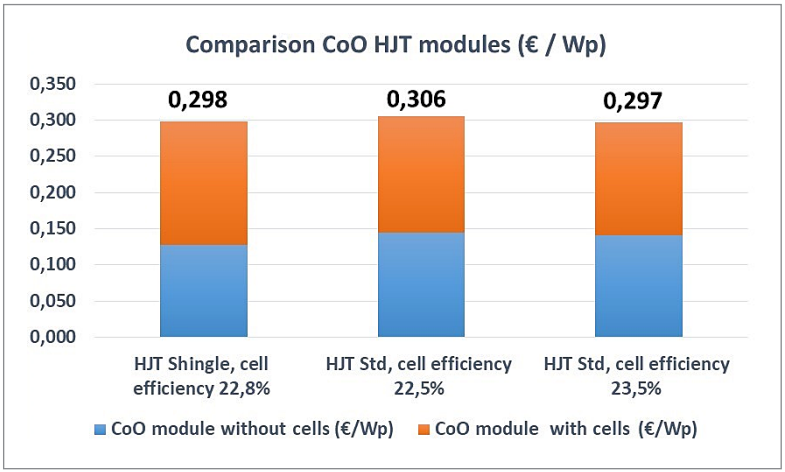


Figure 16. Initial CoO evaluation for SHJ shingle technology. If similar cell efficiencies are considered in order to emphasize just the impact of the bill of materials differences (BOM), shingle technology is shown to remain competitive as the increase in cell cost (linked to the metal cost increase) is compensated at the module level by the reduction in ribbon and ECA consumption. The actual costs are even comparable to those for standard SHJ module integration of higher efficiency cells (up to 23.5% in this calculation).

optimizations and the integration of the fabricated record cell batches, even higher module powers will soon be achieved, paving the way for larger scale exploitation.

Acknowledgement

The authors would like to thank the company Amat-Baccini for the shingle string fabrication, performed in its Italian facility, and all the help in the interconnection optimization. The authors also gratefully acknowledge the support of the European Union through the funded H2020 HighLite project under Grant Agreement No. 857793.

References

[1] Yoshikawa, K. et al. 2017, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%", *Nature Energy*, Vol. 2–5, p. 17032.

[2] Adachi, D. et al. 2015, "Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency", *Appl. Phys. Lett.*, Vol. 107, 233506.

[3] TaiyangNews 2021, "25.2% efficiency for GS-Solar HJT solar cell", Press release [http://taiyangnews.info/technology/25-2-efficiency-for-gs-solar-hjt-solar-cell/].

[4] Favre, W. et al. 2020, "25% efficient large area silicon solar cell: Paving the way for premium PV manufacturing in Europe", *Proc. 37th EU PVSEC* (virtual event).

[5] Gérenton, F. et al. 2020, "Analysis of edge losses on silicon heterojunction half solar cells", *Sol. Energy Mater. Sol. Cells*, Vol. 204, 110213.

[6] Harrison, S. et al. 2020, "Challenges for efficient integration of SHJ based solar cells in shingle module configuration", *Proc. 37th EU PVSEC* (virtual event).

[7] Baliozian, P. et al. 2020, "Postmetallization passivated edge technology for separated silicon solar cells", *IEEE J. Photovolt.*, Vol. 10, No. 2.

[8] Portaluppi, B. et al. 2020, "Insights on cell edge defects impact and post-process repassivation for heterojunction", *Proc. 37th EU PVSEC* (virtual event).

[9] Schulte-Huxel, H. et al. 2019, "Interconnect-shingling: Maximizing the active module area with conventional module processes", *Proc. 9th SiliconPV*, Leuven, Belgium.

[10] Gérenton, F. et al. 2019, "Silicon heterojunction and half-cell configuration: Optimization path for increased module power", *Proc. 46th IEEE PVSC*, Chicago, Illinois, USA.

[11] Kaiser, C. et al. 2020, "Reduction of ECA amount for the ribbon interconnection of heterojunction solar cells", *Proc. 37th EU PVSEC* (virtual event).

[12] Danel, A. et al. 2018, "Silicon heterojunction cells with open circuit voltage over 750mV", *Proc. 35th EU PVSEC*, Brussels, Belgium.

[13] Galiazzo, M. et al. 2014, "Double printing feasibility of 35um printed Ag finger width", *Proc. 29th EU PVSEC*, Amsterdam, The Netherlands, pp. 1387–1391.

[14] Geissbühler, J. et al. 2014, "Silicon heterojunction solar cells with copper-plated grid electrodes: Status and comparison with silver thick-film techniques", *IEEE J. Photovolt.*, Vol. 4, No. 4.

[15] Dabirian, A. et al. 2017, "Metallization of Si heterojunction solar cells by nanosecond laser ablation and Ni-Cu plating", *Sol. Energy Mater. Sol. Cells*, Vol. 159, pp. 243–250.

[16] Fell, A. et al. 2018, "Modeling edge recombination in silicon solar cells", *IEEE J. Photovolt.*, Vol. 8, No. 2, pp. 428–434.

[17] Saint-Cast, P. et al. 2019, "Extracting metal and edge recombination parameters which are compatible with multi-dimensional cell simulations", *Proc. 36th EU PVSEC*, Marseille, France.

[18] Giglia, V. et al. 2020, "Influence of edge recombination on the performance of half-, shingled- and full silicon heterojunction solar cells", *Proc. 37th EU PVSEC* (virtual event).

[19] Roth, J. et al. 2015, "Thermal laser separation (TLS) dicing process study – A new technology for cutting silicon solar cells for high-efficiency half-cell modules", *Proc. 31st EU PVSEC*, Hamburg, Germany, pp. 716–718.

[20] Lewke, D. et al. 2015, "Thermal laser separation – A novel dicing technology fulfilling the demands of volume manufacturing of 4H-SiC devices", *MSF*, Vol. 821–823, pp. 528–532.

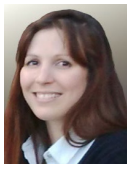
[21] Lelievre, J.F. et al. 2020, "Alternative CZ ingot squaring and half-cell cutting methodology for low-temperature PV cell and module technologies", *Proc. 37th EU PVSEC* (virtual event).

[22] Tune, D.D. et al. 2020, "Measuring and mitigating edge recombination in modules employing cut cells",

Proc. 37th EU PVSEC (virtual event).
[23] Munoz-Rojas, D. et al. 2014, "Spatial atmospheric atomic layer deposition: A new laboratory and industrial tool for low-cost photovoltaics", *Mater. Horiz.,* Vol. 1, No. 3, p. 314.
[24] Richter, A. et al. 2011, "Excellent silicon surface passivation with 5 Å thin ALD Al_2O_3 layers: Influence of different thermal post-deposition treatments", *physica status solidi (RRL)*, Vol. 5, No. 5–6, pp. 202–204.
[25] Portaluppi, B. et al. [forthcoming] "Low temperature post-process repassivation for heterojunction cut-cells".
[26] Carriere, C. et al. 2020, "Toward shingling interconnection with SHJ solar cells", *Proc. 37th EU PVSEC* (virtual event).
[27] Carriere, C. et al. [forthcoming], "Shingle interconnection of HJT solar cells: Reliability study and upscaling for high power PV modules".
[28] Harrison, S. et al. 2021, "400W in shingle SHJ configuration: Promising optimization path for high power modules", *Proc. IEEE 48th PVSC*.
[29] Eymard, J. et al. 2020, "CTMOD: A cell-to-module modelling tool applied to optimization of metallization and interconnection of high-efficiency bifacial silicon heterojunction solar module", *Proc. 9th Worksh. Metalliz.* (virtual event).

About the Authors

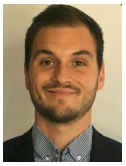
Samuel Harrison obtained his Ph.D. in 2005 in microelectronics, investigating advanced CMOS components, and then worked for Philips Semiconductors on industrial CMOS integration. He joined CEA in 2007, initially involved in microsystems development, before switching to the PV department in 2009. His work has since focused on heterojunction crystalline cells, with a contribution in particular to the ramp-up of the industrial pilot-line, while also leading several research activities on alternative cell concepts.



Carolyn Carriere studied chemistry and materials science at the Aix-Marseille University, and holds an M.Sc. in physics of materials for energy. From 2013 she worked as an engineer at CNRS (France), at the University of Sherbrooke 3IT (Canada) on concentrated PV, and at imec (Belgium) in the thin-films engineering department. She joined the PV module research group of CEA-INES in 2020, to work on innovative module and interconnection technologies.

Vincent Barth received his Ph.D. in 2014 from the Sorbonne University in the field of organic PV, working on the synthesis of small molecules as donor material or as HTL material and their use in PV devices. He joined CEA-INES in 2017 to work on PV module technology. His work focuses on industrial manufacturing of heterojunction modules, with a specific interest in different interconnection solutions.

Dr. Armand Bettinelli received his Ph.D. from Strasburg University in 1987 for his work on cofiring of alumina and tungsten. He joined CEA-INES in 2005, where he holds a senior expert position in cSi solar cell metallization and interconnection. From 2005 he introduced and optimized at CEA the SmartWire and the ribbon-gluing interconnection technologies for heterojunction cells, and more recently shingling, always being mindful of the link between cell metallization and cell interconnection quality.



Baptiste Portaluppi received his M.Sc. in 2019 from the Belfort Montbéliard Institute of Technology (UTBM) with a focus on renewable energy production. He completed his final project assignment at CEA-INES on wafer Si quality in 2019. He currently works as a research engineer on the development of edge repassivation solutions for shingle and half-cell SHJ technology.

Valentin Giglia received his M.Sc. in material science and engineering with a focus on semiconductor materials from the National Institute for Applied Sciences (INSA) in Rennes in 2018, and also his M.Sc. in solid state chemistry from the University of Rennes. He is currently a Ph.D. student at CEA and INL, specializing in the simulation of the impacts of heterogeneities of heterojunction solar cells at the entire cell level.

Marco Galiazzo received his M.Sc. in telecommunications engineering from the University of Padova in 2005. From 2006 to 2008 he worked at a start-up as an optical engineer, developing laser sources for material micro-processing. Since 2008 he has worked for Applied Materials Italy in Treviso as an R&D manager, coordinating research work in the fields of solar cell metallization and module manufacturing.

Enquiries
Samuel Harrison
CEA-INES
50 Av. Du Lac Léman
73370 Le Bourget Du Lac Cedex
France

Email: samuel.harrison@cea.fr
Tel: +33 (0) 479792807