Mechanical strength of HJT cells: Raising the bar in achieving a low wafer thickness in production

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Abstract

The mechanical strength of silicon cells remains one of the main issues in the PV industry, as it requires a balance of conflicting interests between the upstream and the downstream segments. With margins squeezed along the supply chain, cell prices are becoming increasingly under pressure, but the ongoing reduction of wafer thickness raises concerns over the growing risks of production losses and reliability issues. Owing to low-temperature processing, a fully symmetric structure and fewer production steps, silicon heterojunction technology (HJT) is able to tolerate thinner wafers as compared to mainstream passivated emitter and rear cell (PERC) technology. Indeed, the latest achievements in a successful shift from 180µm- to 150µm-thick wafers in mass production of HJT cells gives manufacturers more confidence and brings certain economic benefits. At the same time, however, the rapid scaling-up of the wafer size to M6, M10 and G12 will face immense challenges with regard to a reduction in wafer thickness. The race for higher cell efficiency and greater power output from PV modules of standard dimensions will demand new R&D approaches and equipment suppliers. In this paper, an even greater reduction in wafer thickness, down to 130µm, is evaluated, and the critical steps in terms of breakage rates in cell and module production processes are reviewed. Finally, the mechanical stability and reliability of these thin HJT cells in glass–backsheet and glass–glass module types are addressed.

Introduction

Today silicon heterojunction technology (HJT) holds efficiency records for double-side-contacted [1] and rear-side-contacted [2] Si solar cells fabricated from industrial-size Cz wafers. According to the recent International Technology Roadmap for Photovoltaic (ITRPV) report [3], in mass production, HJT technology yields the highest efficiencies for solar cells with a conventional metallization grid and will continue to hold onto the leading position in efficiency among Si PV technologies until at least 2030 or, in other words, until the development of cost-effective tandem-Si-based technology.

Unfortunately, despite the outstanding efficiency, the market share of HJT solar cells is limited because of higher production costs than for passivated emitter and rear cell (PERC) technology, which recently became mainstream. The higher cost of HJT modules can be offset by the advantages of HJT cells, such as lower temperature coefficient < 0.3%/°C, higher open-circuit voltage ≥ 740mV and greater bifaciality ≥ 90%, providing additional gain in solar module performance via higher output at operating temperature, lower resistivity losses and better harvesting of scattered light arriving at the rear side of bifacial modules. These advantages, however, are usually not so evident for investors. Thus, achieving a decrease in production costs is necessary in order for HJT to increase its market share.

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Like other high-efficiency Si PV technologies, HJT requires n-type monocrystalline silicon (mono Si) wafers, which are now up to 10% more expensive than p-type wafers used in mainstream Si PV technologies [4]. Despite the contribution of Si wafers to the total module costs having a decreasing trend in the last few years, it still constitutes about one-third in the case of monocrystalline wafers. A reduction of the Si wafer thickness is therefore one of the most obvious ways to decrease the costs of HJT modules. Moreover, as the production of mono Si from feedstock to ingots demands more than fifty per cent of the total energy required for solar module production [5], using thinner wafers for HJT cells makes this technology more competitive in the countries which have committed to "making finance flows consistent with a pathway towards low greenhouse gas emissions", within the framework of the UNFCCC Paris Agreement.

The effect of wafer thickness on the HJT cell parameters has recently been studied at the laboratory level and in pilot-line production by various research groups [6–8]. It has been found that, thanks to outstanding amorphous silicon passivation quality providing surface recombination rates as low as 1cm·s^{-1} [8], the increase in open-circuit voltage and the reduction in bulk recombination rate can compensate the effect of a reduction in short-circuit current when using thinner wafers [6]. As a result, there are almost no differences in the efficiencies of HJT

cells manufactured from wafers with thicknesses ranging from 160µm down to 90µm, while maximal efficiencies for cells with optimized light trapping were observed with around 100µm-thick wafers [7]. Such findings are consistent with the data obtained for the cells manufactured on Hevel's production line.

As Hevel completely switched to 150µm-thick c-Si wafers in production as early as 2018 [9], the focus of the study reported in this paper will be on further reductions of wafer thickness. A comparison of the electrical parameters for bifacial cells of different thicknesses is shown in Fig. 1(a). As expected, the transition to a 130µm wafer thickness leads to a reduction in I_{sc} by 0.1A, with a simultaneous increase in V_{oc} by about 2–3mV, as compared to the 150µm wafer thickness, and results in an overall cell efficiency loss of about 0.2%$_{abs}$.

In contrast to the cell data, thinner wafers lead to a power gain at the module level. Fig. 1(b) shows the parameters of the glass–backsheet modules assembled from the HJT cells of different thicknesses. As one can see, the additional absorption of light reflected from the white backsheet compensates the current losses, so that the cell-to-module (CTM) losses become smaller for thinner wafers, with an overall gain of up to 3W for a 60-cell module.

As there is no significant reduction in efficiency at the cell level, the main issues for the implementation of thin Si wafers in mass production are related to the yield losses caused by higher wafer breakage rates, and the lower mechanical strength of the cells affecting a module's long-term durability. This paper presents a brief overview of the experience in using wafers of thicknesses of 150µm and below for HJT cells and the production of modules at Hevel [9,10], followed by a discussion of the general status of related issues.

Mechanical cell strength and production yield losses

Wafer handling at all production steps and the thermal stress induced by cell processing are considered the main reasons for cell breakage during manufacturing. Since HJT cell manufacturing requires fewer production steps

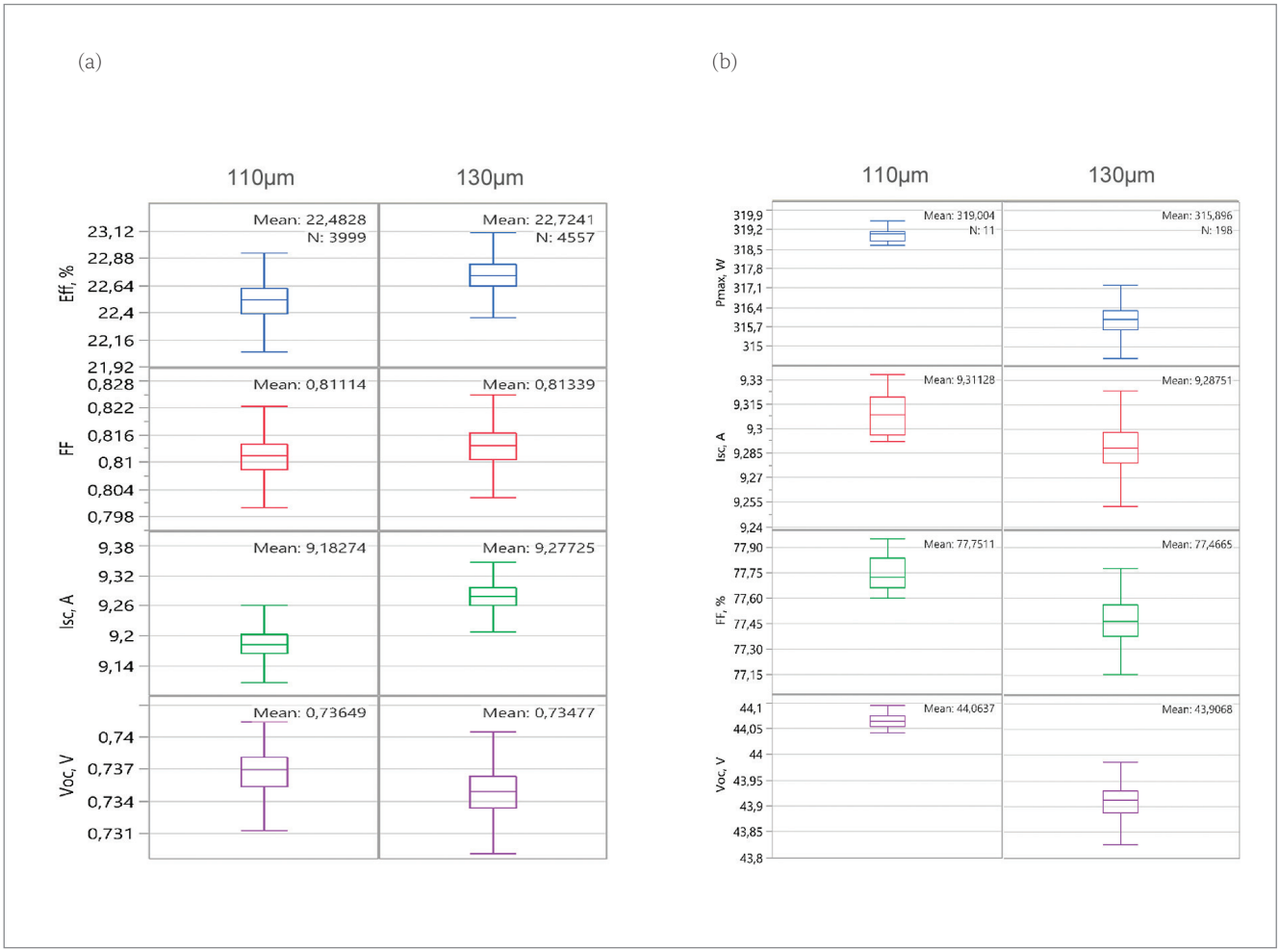

Figure 1. (a) Comparison of the electrical parameters of the HJT cells with thicknesses of ~110 and 130µm, fabricated from wafers with initial as-cut thicknesses of 130 and 150µm, respectively. (b) Comparison of the electrical parameters of the HJT modules assembled from the respective cells. (Note that the results present the state of production in early 2018 and are not representative of the current production level, which is at 23.5 % cell efficiency for 150µm wafers.)

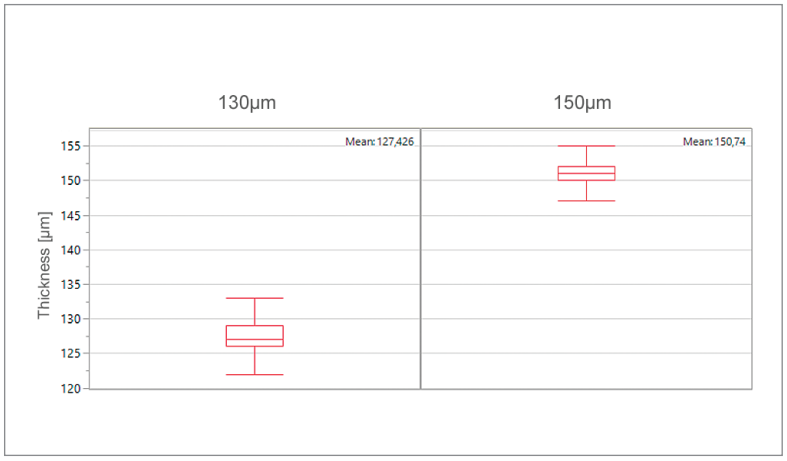

Figure 2. Distribution of the initial n-type c-Si wafer thicknesses used in the HJT production process in this study. The chemical SDE process will further reduce the final cell thickness by approximately 15µm on average, to 115 and 135µm, respectively.

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and much lower processing temperatures than other c-Si technologies, the implementation of thinner and larger crystalline silicon wafers is consequently more favourable for HJT. In practice, however, the implementation of thin wafers requires an assessment of mechanical stability and breakage rate, both of which can only be quantified in actual full-scale production.

Earlier manufacturing tests with thin wafers in a pilot-line production [11] demonstrated that HJT cells with initial wafer thicknesses down to 120µm could be processed using existing automatic wafer-handling systems without dramatically affecting the breakage rate and production yield. Further thickness reduction, however, required manual wafer handling and was therefore not suitable for production. During Hevel's full transition to 150µm c-Si wafers in production in 2018 [9], in general no significant breakage or yield reduction occurred; when the initial wafer thickness was reduced from 180 to 150µm, no major modification to wafer handling and transport systems were necessary. Currently, other HJT cell manufacturers use wafers with initial thicknesses in the range 150 to 170µm [12,13].

In the present study, cell breakage rates were evaluated for initial wafer thicknesses of 150 and 130µm (Fig. 2) for individual HJT processing steps separately, as well as for the loading/unloading and cell-handling steps in a full production environment without modifications of production or handling tools. Wet-chemical saw-damage etching (SDE) and texturing treatment result in a further reduction in thickness by approximately 15µm, and so the final cell thickness decreases to 135 and 115µm on average, respectively.

The breakage rates are presented in Table 1. An analysis of a regular production process with 150µm wafers, averaged over many months and many millions of cells, reveals that the most sensitive step with regard to cell breakage in the Hevel production line is the wafer transport and loading/unloading step, while all other steps together result in a similar breakage rate. Among the latter steps, the highest breakage rate is observed during the metallization step, which is performed by standard screen printing.

A reduction of the c-Si wafer thickness to 130µm, corresponding to final cell thicknesses in the range 110–120µm, increases the breakage rates by a factor of two for wafer handling at the plasma-enhanced chemical vapour deposition (PECVD) step, and by a factor of 1.5–2 at the metallization step, while breakage rates at other steps are virtually unaffected. Nevertheless, the total breakage loss values remain relatively low and do not exceed 0.5% for cells fabricated from 130µm wafers, which leads one to believe that with some modification of the wafer handling system, the breakage rate can be kept under control in production, even for such low wafer thicknesses.

One option for reducing the influence of transport on the cell mechanics during HJT processing is to implement contactless cell-handling systems [14]. At the same time, the screen-printing process should be improved in

Process step	150µm wafer	130µm wafer
Wafer inspection (WIS), including chipped wafers	Breakage and chips 0.03%	0.04%
Wet chemistry	0.01%	0.01% Occasional wafer sticking
Loading/unloading and PECVD	0.1%	0.2%
Physical vapour deposition (PVD)	0.02%	0.02%
Metallization (screen printing)	0.04–0.06%	0.08%
Cell inspection	Breakage and chips 0.02–0.08%	Breakage and chips 0.02–0.08%
Total:	0.22–0.30%	0.37–0.43%

Table 1. Breakage rates for the various HJT production steps and for two different wafer thicknesses of 150 and 130µm. The most critical steps (highlighted by shading) for wafers thinner than 130µm in production are the wafer handling and cell metallization equipment.

Module assembly	GG 72-cell (2.4mm glass)	GG 72-cell (2.4mm glass)	GBS 60-cell (3.2mm glass)	GBS 60-cell (3.2mm glass)
Initial wafer thickness	150µm	130µm	150µm	130µm
Wafer size and format	156×156, full	156×156, full	156×156, full	156×156, full
Interconnection type	ECA, 5 busbars	ECA, 5 busbars	SWCT, 18 wires, Ø 250µm	SWCT, 18 wires, Ø 250µm
Cell breakage rate at interconnection step	0.06%	0.06–0.09%	0.11%	0.2%

Note: GG and GBS represent glass–glass and glass–backsheet module types, respectively.

Table 2. HJT module assemblies used in this study and the cell breakage rates detected at the cell interconnection step for two interconnection techniques (ECA and SWCT) and for two different HJT wafer thicknesses of 150 and 130µm.

order to facilitate further reduction of the cell thickness in production. Besides an advanced screen-printing process, recently proposed contactless printing processes – such as pattern transfer printing [15] or multi-nozzle dispensing [16] – should be considered as alternative solutions for forming the metallization grid on very thin cells.

Interconnection process and module assembly

HJT cells require a low-temperature interconnection process that can be performed via soldering [17], gluing by means of electrically conductive adhesive (ECA) [18,19], SmartWire Interconnection Technology (SWCT) [20], shingling or other techniques. In any case, because of the sensitive cell passivation of a-Si:H, the temperature of the interconnection process is limited to less than 200–240°C. It should be noted that the mechanical stability of the interconnected cells in a module is highly dependent on the properties and type of the interconnection materials, primarily the wire or busbar ribbon thickness, the laminate thickness and so on.

In this study, HJT modules were assembled by means of ECA and SWCT interconnections at Hevel's current production facility. Fully automated equipment was utilized for stringing, busing and other module assembly steps. Table 2 presents the details of the module assemblies. Full cell 156×156mm wafers (M2) were used, along with the two different wafer thicknesses of 150 and 130µm (see above). The former is the current c-Si wafer thickness production standard at Hevel, while the latter is used only for assembling a limited number of modules (~20 per module type) as an initial trial. Glass–glass (GG) and glass–backsheet (GBS) module types were produced in order to assess a broader range of products for thinner cells. Fig. 3 shows examples of the electroluminescence images of the finished modules assembled from thin HJT cells.

The HJT cell breakage rates for the interconnection processes are given in Table 2. For standard 150µm cells, ECA interconnection results in slightly lower cell breakage rates than SWCT interconnection; at the same time, both values remain reasonably low. A reduction of the wafer thickness to 130µm results in much higher breakages for SWCT than for ECA. For SWCT interconnection, the number of thin cell cracks rises by a factor of two, while for ECA it still remains at an acceptable level. Apparently, while the SWCT interconnection allows 150µm wafers, a further thickness reduction will require major modifications to the stringer to allow very thin cells in production. The data therefore highlight the fact that the cell interconnection technology is a crucial step which potentially hinders the use of very thin (<120µm) HJT cells in module production. In particular, it is interesting to postulate whether

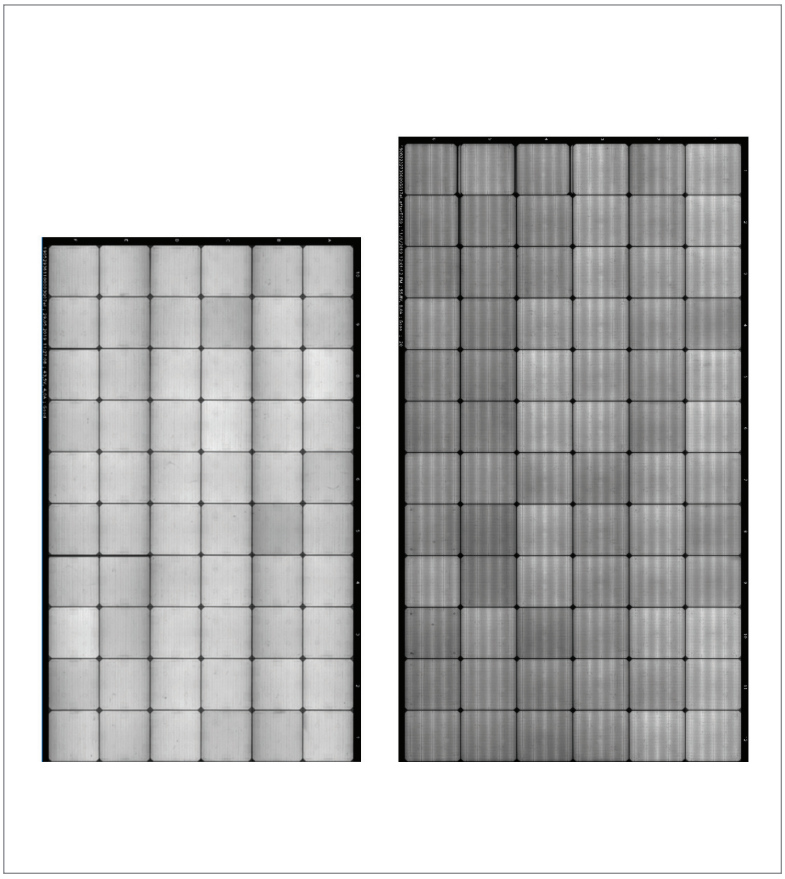

Figure 3. Electroluminescence images of the GBS SWCT-interconnected and GG ECA-interconnected modules assembled from HJT cells with an initial wafer thickness of 130µm.

a multi-busbar (MBB) cell interconnection scheme that is becoming mainstream nowadays will pose similar constraints on the cell thickness to those for SWCT.

HJT module reliability

Cell cracks are one of the most important degradation factors associated with solar modules, especially when thinner cells are considered. Microcracks and chips appearing at different production steps are found to be the main cause of cracks, which can start to propagate over the cell area when thermal or mechanical in-plane tensile stress is induced during module operation. Tensile stress in the cell within a module is strongly influenced by the respective bill of materials (BoM) – glass or backsheet protection cover, interconnection type and wire (busbar ribbon) diameter (thickness), lamination foil thickness, frame design, etc. – as well as by external climatic stress factors.

Several HJT module types (see Table 2) were assembled for laboratory testing with a particular emphasis on cell mechanical stability. As well as the regular tests performed in accordance with the IEC 61215 standard, such as static mechanical load (SML) and climatic (thermocycling/TC, damp heat/DH) tests, extended climatic stress sequences were conducted. These extended tests form part of the forthcoming IEC 63209 standard series – 'Extended stress testing'. In addition, a combined mechanical and climatic stress sequence (SML→DML→TC50→HF10, where DML = dynamical mechanical load), as implemented by several quality programmes other than IEC (e.g. PVEL [21]), was applied. The combined test sequence is believed to be better at reproducing the influence of the interconnection on the mechanical strength of the cells.

Glass–glass (GG) modules were tested in a 72-full cell format and with two different glass thicknesses of 2.4 and 2.0mm; the latter is becoming the mainstream GG product for many module manufacturers. In addition, a 60-cell glass–backsheet (GBS) module was tested. With regard to cell thickness, two different cell types were used, fabricated from 150 and 130µm initial c-Si wafer thicknesses.

GG HJT modules were noted to exhibit excellent mechanical stability of the HJT cells

inside. Indeed, the static mechanical load test performed on many GG modules resulted in zero cell cracks, independently of the cell thickness (150 or 130µm) and glass thickness (2.4 and 2.0mm) used. Generally, the power loss for the GG module after the SML test was well below 1%. Subsequently adding dynamic mechanical loading, followed by climatic stress in a sequence SML→DML→TC50→HF10, results in no cell or interconnection damage, and power degradation still keeps well below 1%. This demonstrates that HJT cells with thicknesses in the range 150 to 130µm can be used in glass–glass module designs without affecting their mechanical stability, provided that an appropriate interconnection scheme and BoM are selected. On the other hand, HJT GBS modules assembled from thin HJT cells exhibited occasional cell cracks under static mechanical tests with maximal loads applied, leading to a power loss ranging from 1 to 4%, depending on the number of cells cracks and cell thickness.

The high mechanical stability of the cells in the GG module is generally believed to be due to the symmetric GG module design, which results in the cells located near the neutral plane coinciding with a zero-stress position, as opposed to GBS modules. Subsequent climatic tests, however, do not affect the module power, as seen in Table 3. To conclude, in terms of module assembly and reliability, a reduction of the HJT cell thickness to 150µm is feasible without significantly affecting breakage rate and module reliability. At the same time, a further reduction of the HJT cell thickness, down to 130µm, will strongly favour GG module technology over the GBS option.

Conclusions

In this paper, Hevel's recent activities on implementing thinner c-Si wafers in the production of HJT solar cells were reviewed. The results demonstrate that the wafer thickness can be reduced to 150µm without affecting production yield, increasing breakage rate and sacrificing module reliability for both glass–backsheet and glass–glass HJT module types. A further reduction of initial wafer thickness to 130µm increases the breakage rate by up to a factor of two during some of the production steps.

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The most sensitive steps are the wafer and cell precursor handling and the metallization process. Consequently, new or modified approaches to wafer handling that minimize the impact on the cells are required, one of them being contactless wafer transport, for example. The most crucial process that limits the use of very thin (<130µm) wafers in HJT module production is cell interconnection. While it was shown that ECA-type interconnection appears to be the least damaging in the assembly of high-quality modules, the breakage rate could still be minimized by modifying the existing process.

Finally, it was shown that, in terms of module reliability, very thin cells are best assembled in a glass–glass module type, which allows protection of the cells from cracking under different climatic stress factors. To conclude, it is believed that a c-Si wafer thickness reduction to at least 130µm should be possible for an industrial HJT process, provided that the modifications in production equipment are thought through and implemented. As monocrystalline silicon is the most energy-consuming step in the PV module production chain, the use of thinner wafers gives the HJT process a clear advantage with respect to other Si crystalline technologies in terms of lower levels of greenhouse gas emissions.

Module assembly/ Test sequence	GG 72-cell (2.4mm glass)	GG 72-cell (2.0mm glass)	GBS 60-cell (3.2mm glass)	GBS 60-cell (3.2mm glass)
Wafer thickness [µm]	130/150	150	150	130
SML (load: 5,400/2,400Pa)	0.2% No cell cracks	0.2% No cell cracks	1–2% Occasional cell cracks	1–4% Frequent cell cracks
Mechanical stress sequence in accordance with PVEL (SML→DML→TC50→HF10)	0.6% No cell cracks	0.6% No cell cracks	1.3% No new cracks after climatic tests	2–4% No new cracks after climatic tests
TC600	<1.5%	<1.5%	≈2%	≈2%
DH2000	≈0%	≈0%	≈2%	≈2%

Note: SML = static mechanical load, DML = dynamic mechanical load, TC50 = 50 thermocycles, HF10 = 10 humidity–freeze cycles, TC600 = 600 thermocycles, DH2000 = damp heat for 2,000h.

Table 3. Results of reliability tests for the HJT modules with cells of different thicknesses and for different module types. The degradation is shown in % of initial power for individual or sequential tests. The individual tests are performed in accordance with IEC 61215.

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