Industrial n-type PERT cells with doped polysilicon passivating contacts: Past, present and future

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Abstract

The industrial n-type passivated emitter and rear totally diffused (PERT) cell with doped polysilicon passivating contacts is an attractive next-generation technology, as average efficiencies above 24% have recently been demonstrated in mass production. Despite these very promising efficiencies, several factors are limiting this technology's rapid adoption in mass production, including the relatively higher cost of manufacturing equipment and the increased process complexity, leading to lower manufacturing yields. This paper provides a short overview of historical developments, presents the main approaches in mass production today, discusses potential process simplifications, and briefly touches upon a key topic for the future, namely reducing the silver (Ag) consumption per cell.

Introduction

Since 2014, the crystalline silicon (c-Si) PV industry has experienced a learning rate (LR) of over 25%, meaning that the manufacturing cost (in $/W) of PV modules has decreased by over 25% for every doubling of the cumulative production. As explained in detail in Chen et al. [1], this accelerating LR is due to several factors, including the massive scaling-up of manufacturing, mainly in China, rapid improvements in cell and module efficiencies, and a strong alignment between the players around a domestic supply chain for high-throughput tools and key materials (polysilicon, wafers, Ag pastes, glass, etc.).

Although China has been a major contributor to the rapid development of PV manufacturing, it does not mean that PV manufacturing outside China cannot be competitive. This is because high labour costs are becoming less significant with increased automation and throughput, while shipping costs are becoming proportionally more important with falling manufacturing costs and the increasing relevance of factors such as CO_2-footprint [2]. Furthermore, PV manufacturing is becoming a strategic industry for ensuring a domestic supply of low-cost and sustainable energy, and for creating thousands of jobs across the value chain.

The upshot of all this is a renaissance of PV manufacturing in all major PV markets (Europe, USA, India, etc.). For 2021, BloombergNEF analysts are forecasting global PV installations to increase from 132GW in 2020 to somewhere in the range of 160 to 209GW, and standard PV modules prices to fall by a further $0.02/W, to $0.18/W [3]. Consequently, higher solar cell efficiency has never been so important as it is today, since it impacts the manufacturing cost (in $/W) of every other component. Similarly, higher module efficiency is key to reducing the overall PV system costs and ultimately to achieving a lower levelized cost of electricity (LCOE) [4].

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Most c-Si PV modules being sold today are based on gallium-doped (p-type) industrial passivated emitter and rear cells (PERCs) with local aluminium doping [5]. The average efficiency of industrial PERC in mass production has been improving steadily by ~0.5%$_{abs}$ per year, from ~20% in 2013 to ~23% today (see Fig. 1), thanks to hundreds of small improvements in materials, equipment and processing. PERC efficiencies of ~23.5% appear feasible in the coming years, as already demonstrated by Hanwha Q-cells at the pilot-line level [6]. However, progress beyond 23.5% is expected to be slower and more laborious, as explained in several roadmaps [5,7–9].

In parallel to improving PERC efficiency, the PV industry has recently embarked on making several rapid changes in cell and module design in order to increase module power, reduce cell-to-module losses, decrease manufacturing costs and improve energy yield. These changes include:

- Rapid push towards larger wafer formats (up to 210mm).
- Reduction of interconnection losses by cutting cells in half or smaller pieces and introducing multi-busbar concepts.
- Reduction (or even elimination) of cell gaps to improve packing density.
- Introduction of bifacial cell and module designs to collect light from both sides.

As a result of all these changes, the typical efficiency of monofacial PERC modules has quickly improved from 18–19% in 2018 to 20.5–21.5% today, while the

best bifacial PERC modules now have efficiencies in the range 20.4–21.3%.

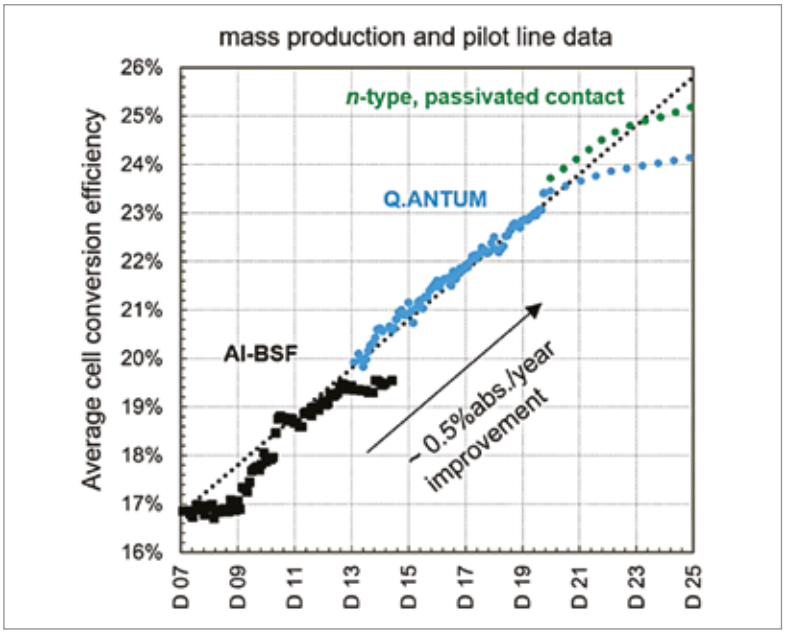
With the progress in PERC cell efficiency expected to be more tedious and major improvements in module design being implemented, next-generation cell technologies capable of efficiencies well above 24% will be required in order to push average module efficiencies above 22%. Several technologies – including passivated emitter and rear totally diffused (PERT), silicon heterojunction (SHJ), interdigitated back contact (IBC) and, more recently, perovskite/silicon (Pk/Si) tandem – have been on the radar of the International Technology Roadmap for Photovoltaic (ITRPV) and of the R&D community for several years [10,11].

Among those technologies, n-type SHJ and n-type PERT with doped polysilicon (poly-Si) passivating contacts seem to be gaining the most traction among PV manufacturers, as average efficiencies above 24% have recently been demonstrated in mass production, while record efficiencies around 25% have been achieved in pilot lines [12–15]. Both of these technologies rely on the concept of carrier-selective contacts to improve cell efficiencies [16] and reduce temperature coefficients [17]. Moreover, both technologies typically feature narrow Ag grids on both sides, resulting in higher bifaciality values than with PERC.

Finally, the use of high-quality phosphorus-doped (n-type) substrates helps to drastically reduce the magnitude of light-induced degradation (LID) and light- and elevated temperature-induced degradation (LeTID) [18]. The combination of lower temperature coefficients, higher bifaciality and lower LID/LeTID enables substantial improvements in the energy yield of a PV system.

Compared with n-type SHJ technology, a major benefit of n-type PERT cells with poly-Si passivating contacts is their compatibility with conventional high-temperature processing, including diffusion, plasma-enhanced chemical vapour deposition (PECVD) of hydrogenated silicon nitride layers (SiN_x:H), firing-through of Ag pastes, and standard soldering of flat ribbons or wires. This allows one to benefit from gettering and hydrogenation to significantly improve bulk lifetimes [19,20]; it also enables manufacturers to tap into a well-established supply chain for equipment/materials and a talent pool that is familiar with high-temperature processing.

On the other hand, there are several factors that limit the rapid adoption of n-type PERT cells with poly-Si passivating contacts. These constraints include the relatively higher cost of manufacturing equipment, the increased process complexity, leading to lower manufacturing yield, and the higher Ag consumption per cell than that for p-type PERC. Note that the relatively higher cost of n-type substrates can also be an additional factor, but this can be mitigated by moving to thinner substrates than for p-type cells [21].



Source: Fath et al. [66].

Figure 1. Average cell conversion efficiencies achieved at Hanwha Q-cells since December 2007 with Al-BSF and subsequently with Q.ANTUM (PERC) technology. The values beyond 2021 represent projections based on internal roadmaps.

Several PV manufacturers are now adding significant production capacity for n-type PERT cells with poly-Si passivating contacts, as significant progress has been made in the last few years on all fronts (materials, equipment, process simplifications). This paper briefly reviews historical developments, examines the main approaches in mass production today and presents potential process simplifications. A key challenge for the future – the reduction of Ag consumption per cell – is also discussed.

Historical developments

The idea of implementing doped poly-Si passivating contacts to improve carrier selectivity in silicon devices is not new. A short overview is given in Fig. 2 and in the paragraphs below. A more detailed overview can be found in a recent review by Hermle et al. [22].

Originally used as an emitter in heterojunction transistors [23], the doped semi-insulating polysilicon (SIPOS) approach enabled impressively high open-circuit voltages (V_{oc}) of 720mV to be achieved on p-type in 1985 [24]. However, approaches based on doped poly-Si have fallen out of favour with most research groups because of the high process complexity and the narrow process window. In 2005, Swanson stated that new contacts with a "J_o of less than 5fA/cm² that make good majority carrier contact" were needed, one for electrons and one for holes [23]. Not long after, SunPower successfully implemented passivating contacts in its Maxeon GEN3 IBC cells, with the V_{oc} improving from 680–690mV (GEN_2) to 710–730mV (GEN3) [25]. Continuous improvements allowed SunPower

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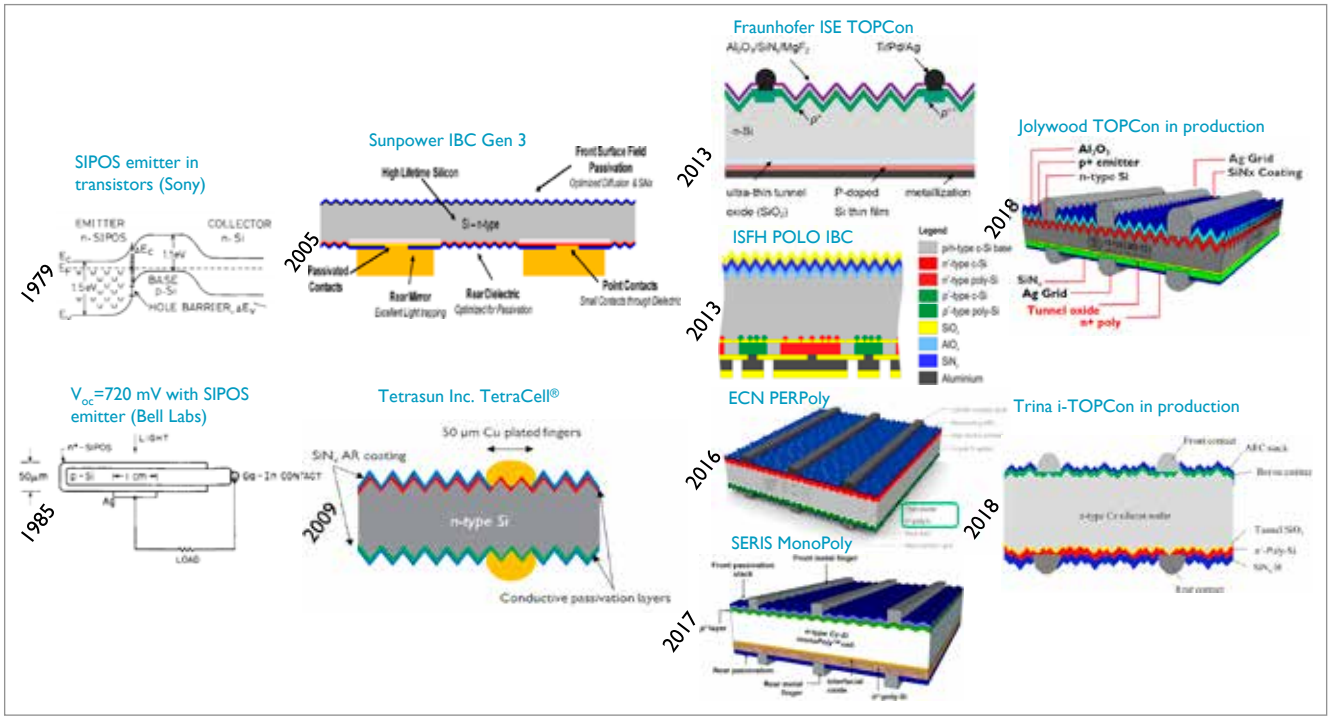

Figure 2. Short overview of the historical developments of poly-Si passivating contacts, leading to high-volume production of n-type cells with tunnel oxide passivated contact (TOPCon) technology.

to demonstrate, in 2016, IBC cells with a total area efficiency above 25% (V_{oc} = 737mV, J_{sc} = 41.33mA/cm^2, *FF* = 82.7%) [26].

In 2009, TetraSun began the development of its TetraCell, featuring conductive passivation layers and Cu-plated contacts on both sides [27]. After its acquisition by First Solar, TetraSun's technology was transferred into production. Median efficiencies of 21.9% (V_{oc} = 701mV, J_{sc} = 39.3mA/cm^2, *FF* = 79.5%), and a best cell efficiency of 22.8% (V_{oc} = 718mV), were demonstrated in 2016 [28]. In the same year, however, the TetraSun line ceased production, as First Solar decided to concentrate on its core thin-film business.

The interest in doped poly-Si passivating contacts exploded when Fraunhofer ISE and ISFH started to report very swift progress in their tunnel oxide passivated contact (TOPCon) and polysilicon on oxide (POLO) IBC concepts, using laboratory processes (photolithography patterning, 2×2cm^2 designated cell area, etc.) and materials (float-zone (FZ) silicon, evaporated contacts, etc.). Fraunhofer ISE introduced its TOPCon technology in 2013 [29]. Initially, a best cell efficiency of 23.7% (V_{oc} = 703mV, J_{sc} = 41.0mA/cm^2, *FF* = 82.2%) was obtained using a homogeneous p$^+$ emitter at the front and a rear passivating contact stack consisting of a 1–2nm chemical oxide, 20nm-thick n$^+$-doped poly-Si, and evaporated Ag. Continuous developments and the implementation of a selective p$^+$ emitter structure at the front led to 25.1% efficiencies in 2015 [30]. Further optimization culminated in Fraunhofer ISE reporting, in 2020, efficiencies of up to 25.8% on n-type FZ, and of even up to 26% on p-type FZ, which is the current world record for two-side-contacted cells, thanks to lower surface recombination and lateral transport losses [31].

ISFH started to develop processes to form n$^+$- and p$^+$-doped POLO also around 2013 [32]. Several years of development led to ISFH announcing in 2018 a POLO IBC on p-type FZ with an efficiency of 26.1%, which remains the world record for a p-type Si solar cell to date [33]. The process to form POLO contacts in these cells consisted of:

1. A dry oxidation to grow a 2.2nm-thick oxide.
2. Low-pressure chemical vapour deposition (LPCVD) of amorphous Si (a-Si).
3. Phosphorus and boron implantations (to form n$^+$ and p$^+$ regions respectively).
4. Annealing above 1,000°C to break up the oxide layer and form contacts between the poly-Si and c-Si via pinholes.
5. Evaporating aluminium (Al).

To bridge the gap between laboratory and high-volume manufacturing, many R&D institutes and companies started to develop methods to implement poly-Si passivating contacts using low-cost materials, equipment and processing steps. In 2016, ECN was among the first to report large-area (6") bifacial n-type PERT cells [34]. ECN's PERPoly cells featured 200nm-thick n$^+$ poly-Si passivating contacts on the back side, formed by means of industrial LPCVD and $POCl_3$ diffusion equipment from TEMPRESS, and screen-printed fire-through Ag contacts on both sides. This was quickly followed by SERIS, who explored both industrial LPCVD and PECVD approaches to form the n$^+$ poly-Si in MonoPoly® bifacial n-type PERT cells.

Contact formation using fire-through Ag pastes was initially challenging, as the pastes partly consumed the n$^+$ poly-Si layers, leading to relatively high recombination current densities in

the metallized areas ($J_{o,met}$) of 386fA/cm² and non-optimum specific contact resistivities (ρ_c) of around 3–5mΩ·cm² [35]. The rapid development of dedicated Ag pastes allowed this issue to be addressed, with excellent $J_{o,met}$ ~ 35fA/cm² and ρ_c ~ 1–2mΩ·cm² values reported only two years later by different authors [36]. By 2018, Meyer Burger in collaboration with SERIS reported 6" bifacial n-type PERT cell efficiencies of up to 22.6% with V_{oc}~700mV using a single piece of inline PECVD pilot-line equipment to form the tunnel oxide and deposit n⁺-doped Si prior to recrystallization in a tube furnace [37].

Around the same time, several companies (Jolywood, Trina Solar, LG and REC among others) started mass production of (6") bifacial n-type PERT with poly-Si passivating contacts by retrofitting old lines and adding only a few new tools to save on capital expenditure (CAPEX) and compete with low-cost bifacial PERC products. Two early examples are shown in Fig. 2, with Jolywood choosing to upgrade several standard n-PERT lines using a LPCVD + phosphorus implantation + tube annealing approach to form the n⁺ poly-Si [38], and with Trina Solar choosing to upgrade a p-type multi Al-BSF line using a LPCVD + $POCl_3$ diffusion approach to form the n⁺ poly-Si [39].

Approaches in mass production today

Today several companies are mass producing n-type PERT cells and modules with passivating contacts [36,37,40,41]. In addition, a number of Tier 1 producers have earmarked existing p-PERC production lines for a future upgrade to TOPCon to limit CAPEX [39]. Like the beginnings of p-type PERC mass production around 2014, the biggest challenge for the industrialization of n-PERT with poly-Si passivating contacts is to find the right process sequence and associated set of tools/materials leading to high efficiency, high yield and low manufacturing cost.

In Fig. 3, the main processing steps for n-PERT cells with poly-Si passivating contacts using different approaches based on LPCVD, PECVD, APCVD or PVD of a-Si are schematically compared, alongside a reference process sequence for bifacial p-PERC. For total cost of ownership (TCO) and LCOE comparisons, the reader is referred to the excellent work recently published by Kafle et al. [42], who compared slightly different approaches to the ones listed in Fig. 3.

The reference bifacial p-PERC process starts with texturing, typically in a batch tool, prior to emitter formation in a $POCl_3$-based low-pressure tube furnace. This is usually followed by a laser processing step to form a selective emitter (SE) and reduce contact recombination losses [8]. This step is listed as optional, as some companies have developed a leaner and more cost-effective process without SE (for one example, see Altermatt et al. [5]). Next, rear emitter removal and chemical edge isolation are achieved by means of single-side etching (SSE) in an inline tool, which also removes the phosphosilicate glass (PSG) and cleans wafers prior to subsequent processing. This can be followed by an optional dry oxidation in a tube furnace to improve passivation and contacting [43]. Typical alternatives include chemical oxidation (either in the SSE tool or separately) or plasma oxidation which can be combined with the subsequent deposition of all passivation layers in a so-called *3-in-1* inline PECVD tool [44]. The exact deposition sequence for the AlO_x/SiN_x passivation layers at the rear and the single-layer (or multi-layer) SiN_x at the front depends on the equipment chosen (PECVD, PEALD, ALD, APCVD). Finally, local laser contact openings (LCO) are formed prior to the metallization sequence, which typically consists of multiple screen-printing steps (rear Ag pads, rear Al grid, front Ag grid), fast-firing in a belt furnace, and a hydrogenation step to reduce the impact of LID and LeTID.

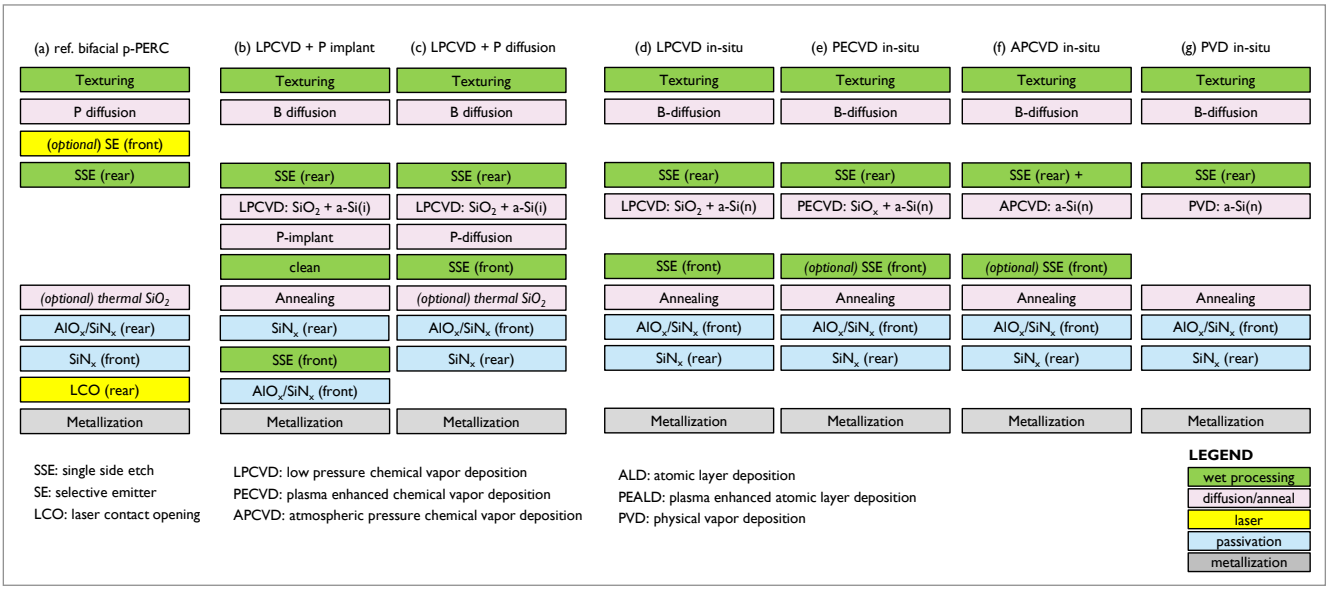

Figure 3. Main cell processing steps for (a) reference bifacial p-type PERC, (b–c) mainstream n-PERT with poly-Si passivating contacts (TOPCon) in mass production, and (d–g) other approaches used in mass production or being evaluated in R&D. The same legend colour code as in Kafle et al. [42] has been chosen, to help with direct comparisons.

"LPCVD is the most mature approach today for the mass production of n-PERT with poly-Si passivating contacts."

The approaches initially used by Jolywood and Trina Solar to mass produce their TOPCon cells are shown in Fig. 3(a) and Fig. 3(b), respectively. Both start with texturing, p^+ diffusion (typically in a BBr_3-based low-pressure tube furnace), and rear SSE in inline tools similar to those for p-PERC. The borosilicate glass (BSG) formed during p^+ diffusion is typically kept intact during the rear SSE step to protect the p^+ emitter during the subsequent front SSE of poly-Si. An LPCVD tube furnace is used to form a thin (1–2nm) tunnel oxide by in situ dry oxidation at low temperatures and to deposit a thick (100–200nm) layer of a-Si. The LPCVD a-Si layer properties are influenced by deposition pressure, silane (SiH_4) concentration and, most significantly, deposition temperature [45].

LPCVD a-Si deposition is followed by n^+ ion implantation (P implantation) at Jolywood (since it retrofitted existing n-PERT lines using P implantation) and $POCl_3$-based diffusion at Trina Solar (since it retrofitted exiting Al-BSF lines using this tool). The P implantation step presents the advantage of being truly single sided, which helps to obtain good reverse-current (I_{Rev}) characteristics and allows, after rear SiN_x deposition, the use of standard inline or batch cleaning tools for the front SSE of poly-Si (undoped). On the other hand, P implantation suffers from limited throughput and requires additional cleaning and annealing steps to form the n^+ poly-Si. The $POCl_3$-based diffusion allows the formation of the n^+ poly-Si in a single high-throughput step, but requires a dedicated tool for the front SSE step, typically using a sequence of alkaline etching (to remove n^+ poly at the front and the edges) and cleaning steps that is critical to achieving high performance and good I_{Rev} characteristics.

Surface passivation typically consists of Al_2O_3/SiN_x at the front and SiN_x at the rear, with the exact layer composition and deposition sequence depending on the set of equipment chosen (as with p-PERC). Finally, the metallization sequence (and equipment required) is typically the same as that for p-PERC, with the exception that Ag grids are printed on both sides. As with p-PERC and n-SHJ cells, several R&D institutes and companies have reported significant efficiency gains when using an extra hydrogenation step after the fast-firing process on TOPCon cells [46,47]. Consequently, the extra hydrogenation step is increasingly becoming standard in all high-efficiency Si cell concepts prior to testing/sorting.

As just explained, LPCVD is the most mature approach today for the mass production of n-PERT with poly-Si passivating contacts. Major advantages of LPCVD include:

- The availability of industrially-proven high-throughput tools from multiple vendors.
- Good thickness control along the wafer and the boat.
- Pinhole-free layers.
- The option of easily creating constant doping profiles using in situ doping (see next section).

On the other hand, LPCVD poses several challenges, such as:

- Lower deposition rates (r_{dep}) than with PECVD or PVD.
- The need for a front SSE step, as the deposition is inherently performed on all wafer sides.
- Deposition on the sidewalls, leading to the risk of tube cracking (hence requiring frequent tube replacements).
- Difficulties in creating a very uniform tunnel oxide along the wafer, which is critical to achieving uniform lifetimes and control carrier selectivity.

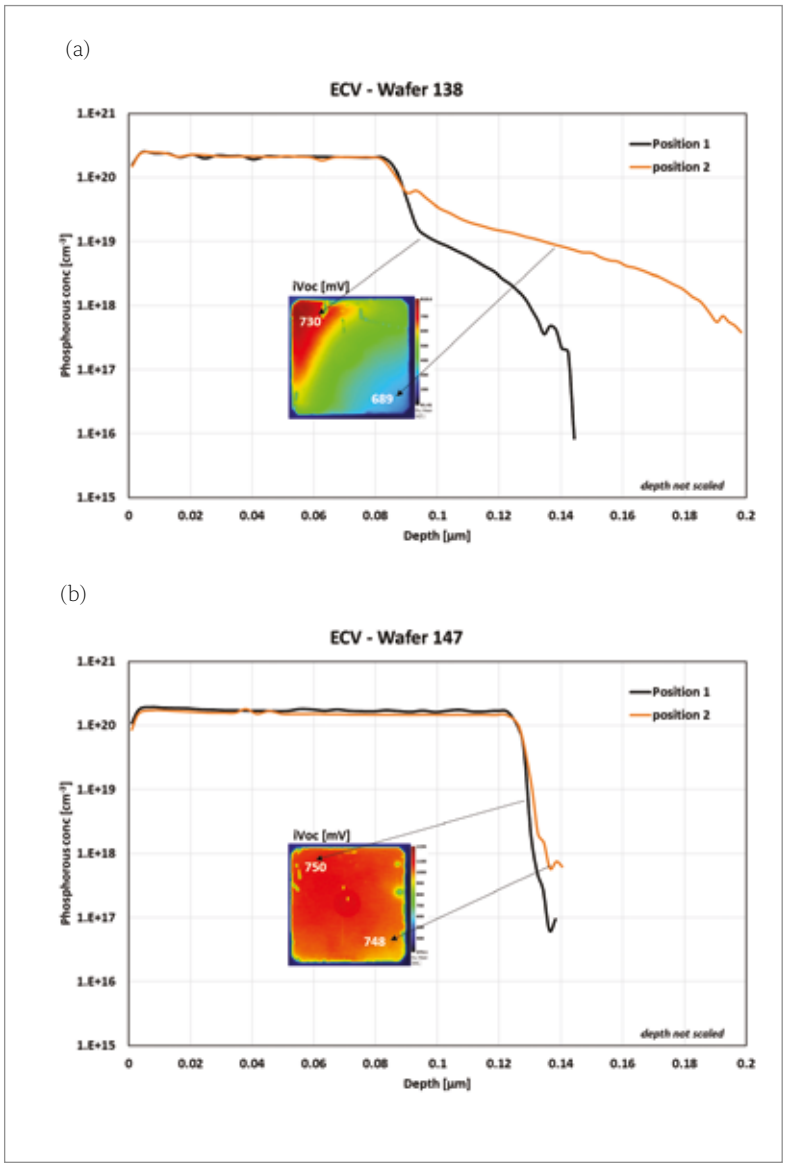

Figure 4. Electrochemical capacitance–voltage (ECV) of n^+ poly-Si layers formed at imec using LPCVD for in situ dry oxidation + a-Si deposition and $POCl_3$ ex situ doping: (a) non-optimized dry oxidation recipe, leading to n^+ tail diffusion and non-uniform iV_{oc} (as shown in the photoluminescence (PL) image insert); (b) optimized dry oxidation recipe, resulting in uniform ECV profiles and iV_{oc} along the wafer.

An example of LPCVD is shown in Fig. 4, where non-optimized in situ dry oxidation led to phosphorus tail diffusion, causing increased Auger recombination losses and hence lower iV_{oc}. This was correlated to thinner oxide formation at the bottom of the M2-format wafer (sitting in a diamond-shaped boat) than at the top. Such non-uniformity issues are highly dependent on the recipe used and the LPCVD tool design (boat, etc.), and are expected to become worse for larger format wafers (M10, G12 formats).

Potential process simplifications

An initial potential process simplification that is being considered is the addition of n^+ doping gas (PH_3 diluted in N_2) during LPCVD. A major benefit of performing LPCVD doping in situ is that the subsequent P diffusion is no longer required. While a post-annealing is still considered to be necessary for achieving high carrier selectivity [48], it allows the elimination of the optional oxidation step prior to passivation (cf. Fig. 3(d) and 3(c)) by adjusting the post-annealing ambient conditions. Moreover, the n^+ poly-Si properties (active doping, thickness, etc.) can simply be tuned by adjusting the LPCVD in situ and post-annealing recipes. An example of this is shown in Fig. 5, where the active doping ($N_{D,act}$) of LPCVD in situ doped n^+ poly-Si layers is simply controlled by changing the PH_3 flow [49]. A major challenge with LPCVD in situ doping is obtaining a sufficiently high r_{dep} and $N_{D,act}$ at the same time. Nevertheless, by adjusting the deposition parameters it is possible to simultaneously achieve an r_{dep} of 4.7nm/min and an $N_{D,act}$ of 1.3E20cm^{-3} [48], which are of the same order as the results reported by Stodolny et al. for LPCVD ex situ [45].

A second potential process simplification that is being considered by a number of institutes and companies is the use of a process sequence based on PECVD in situ (see Fig. 3(e)). It has already been explained briefly that Meyer Burger together with SERIS reported in 2018 a 22.6% n-PERT cell efficiency using a single piece of inline PECVD equipment to form the tunnel oxide (by plasma oxidation) and deposit n^+-doped Si prior to recrystallization in a tube furnace [37]. Major benefits of this approach include:

- Tunnel oxide thickness uniformity is easier to control than in a tube furnace.
- High deposition rates >1.5nm/s can be achieved.
- Layer properties can easily be tuned by adjusting deposition parameters (e.g. temperature, gas flows, pressure, plasma power).

One of the major challenges with inline PECVD at low temperatures is to avoid blistering in thick layers (typically >100nm is required to obtain low $J_{0,met}$ with firing-through Ag metallization) because of the inherently high hydrogen concentration in the deposited a-Si layer. Solutions to this include using additional gases during the deposition process (such as CH_4, NH_3 or N_2O) to incorporate small amounts of carbon (C), nitrogen (N) or oxygen (O) and improve the blistering behaviour [50,51]; however, this also impacts the electrical properties of the layers (bandgap, active doping, mobility, etc.), which can make optimization difficult. Another option is simply to design the inline PECVD equipment to allow depositions at temperatures above 500°C, as already done by Meyer Burger [37] and shown recently by others [52]. In a similar approach, it is also possible to modify tube PECVD equipment to deposit thick and uniform a-Si(n) at high temperatures, with cell results >23% recently demonstrated by Feldmann et al. [53].

One major advantage of tube PECVD is that it is used extensively in the crystalline PV industry for the deposition of passivation layers (AlO_x, SiN_x, etc.) at high throughputs and low cost. Compared with inline PECVD, it might be more challenging to implement uniform plasma oxidation to form the tunnel oxide with tube PECVD, and hence companies might instead choose to perform chemical oxidation during the rear (SSE) step before PECVD. Avoiding wrap-around of a-Si(n) layers is considered a major technological milestone for both inline PECVD and tube PECVD manufacturers, as this would allow the front SSE step to be skipped.

A third process simplification option is to use inline atmospheric pressure chemical vapour deposition (APCVD) to deposit doped a-Si layers at high throughputs. The main benefit of APCVD compared with LPCVD or PECVD is that the deposition is done at atmospheric pressure and hence it works without gate chambers (only gas curtains), vacuum chambers (no pumps) or plasma sources. The basic idea for the

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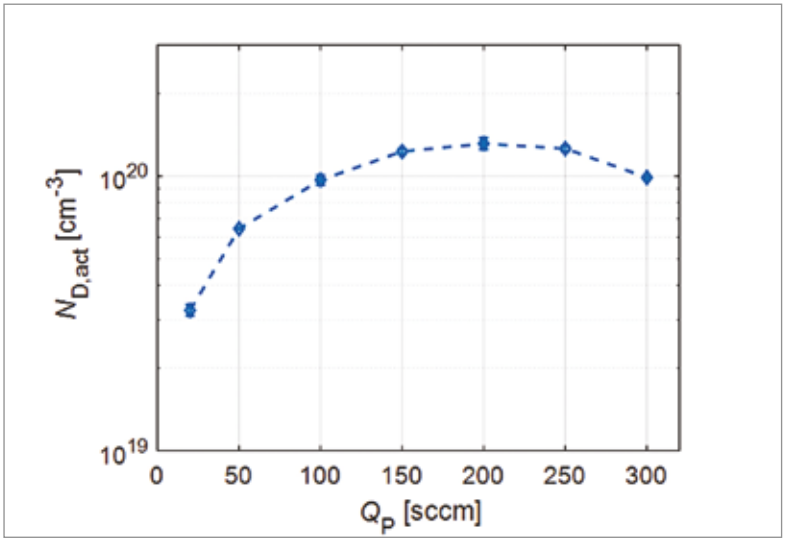


Source: Firat et al. [49].

Figure 5. Active doping (from Hall measurements) of LPCVD in situ doped n^+ poly-Si as a function of PH_3 flow (Q_P).

deposition of a-Si layers is the thermal dissociation of SiH_4 in an atmosphere with very low oxygen concentration (hence the use of N_2 gas curtains), and the precipitation of the silicon atoms as a-Si on the heated wafer. By adding doping precursors (PH_3, B_2H_6, etc.) in the SiH_4 flow it is possible to deposit doped a-Si(n) and a-Si(p) layers, as reported by Merkle et al. [54]. As with inline PECVD, the move to larger format wafers (M10, G12) could possibly be easier with APCVD than with LPCVD. One major challenge is designing the injector heads to achieve uniform and high-throughput deposition without clogging (particularly as the presence of even small amounts of oxygen can lead to silica powder formation). As in the case of PECVD, avoiding any wrap-around deposition is considered a major milestone that is needed in order to skip the front SSE step. Presumably, APCVD is already in use by companies such as SunPower or LG to mass produce IBC cells with passivating contacts. It remains to be seen if APCVD will gain significant market share in the mass production of n-PERT cells with poly-Si passivating contacts.

A fourth simplification option is to use inline physical vapour deposition (PVD) to deposit doped a-Si layers at very high throughputs. Inline direct current (DC) PVD is already used extensively for the deposition of transparent conductive oxides in SHJ cells, with the latest equipment capable of throughputs greater than 10,000 wafers per hour with M6 wafers, or greater than 6,000 with G12 wafers [55]. Apart from the very high throughput capability, major advantages of PVD include:

- Excellent thickness uniformity.
- Solutions already exist for achieving single-side deposition without any wrap-around.
- No hazardous gases (SiH_4, H_2, PH_3, B_2H_6, etc.) are required, unlike with other techniques.

PVD, however, is still a relatively novel technology for forming poly-Si passivated contacts. Excellent results have been demonstrated using laboratory techniques, such as radio frequency (RF) co-sputtering of undoped silicon and boron targets [56] or electron beam (EB) co-evaporation from silicon and gallium phosphide effusion sources [57]. As regards the more industrial approach of performing high-speed DC sputtering from a single P-doped silicon target, results obtained so far have been limited to iV_{oc} < 700mV as a result of insufficient dopant activation, the difficulties in procuring Si targets with a dopant density well above 1E20cm^{-3}, and possibly some sputtering damage [58].

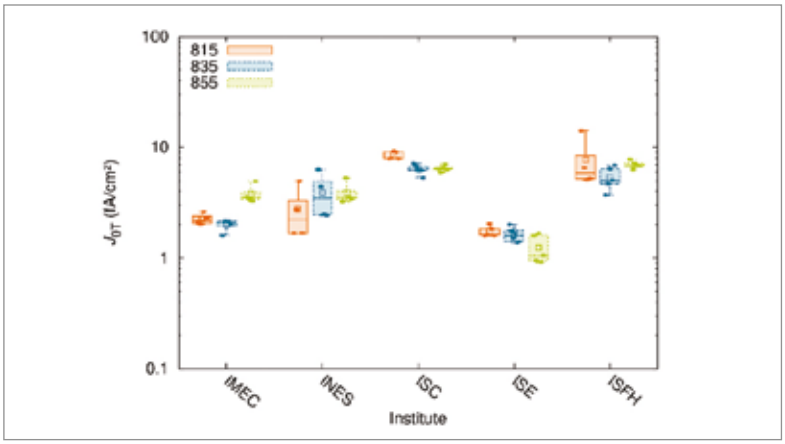
Overall, there is an enormous potential for process simplifications (and associated CAPEX reductions) in the mass production of n-PERT cells with poly-Si passivated contacts. Excellent progress has already been made using the various approaches listed above, and other promising depositions techniques, such as plasma oxidation and plasma-assisted in situ doping deposition (POPAID) or plasma-enhanced atomic layer deposition (PEALD), are also being investigated to form n^+ poly-Si layers. For example, Jolywood recently reported excellent cell results >24% with yields >97% using its new POPAID technology in pilot lines [59]. This technology has the potential to drastically reduce the CAPEX required for new lines, bringing it on par with (or below) that needed for bifacial p-PERC while enabling significantly higher cell efficiencies. In a joint experiment involving different approaches (LPCVD ex situ, LPCVD in situ, PECVD in situ) to form n^+-doped TOPCon layers (tunnel oxide, n^+ poly-Si, dielectric capping) in industrial tools, all the partners were able demonstrate excellent $J_{o,total}$ (see Fig. 6), $J_{o,met}$ and ρ_c values using screen-printed Ag contacts [60]. This clearly shows that the equipment and know-how to produce >24% n-PERT cells with poly-Si passivated contacts are quickly maturing. This is expected to lead to a rapid reduction in CAPEX and manufacturing costs in the coming years because of increased competition across the supply chain, similar to what happened with p-PERC between 2014 and 2018 [1].

Approaches to reducing Ag consumption

One of the major challenges for cost-effective manufacturing of PV modules is to reduce Ag consumption, as it now represents 10% of the overall module cost structure [61]. This is expected to get worse as annual PV production ramps up towards the terawatt level by the end of the decade [62]. According to the latest version of the ITRPV 2020 [10], the median consumption value in 2020 was 90mg of Ag per cell (G1 format), representing 17mg/W (assuming a median 21% efficiency based on Al-BSF and PERC market shares in 2020). As a result, the 132GW of PV modules produced in 2020 consumed at least 2,244 tonnes of Ag or about 9% of the global Ag production.

The PV annual consumption of Ag is expected to increase because: 1) the quantity of PV modules produced per year is increasing faster than manufacturers can reduce Ag consumption per cell; and 2) higher efficiency concepts, such as TOPCon

"Ag consumption now represents 10% of the overall module cost structure."



Source: Fellmeth et al. [60]

Figure 6. Total dark recombination current density $J_{o,total}$ for an n-type bulk and two unmetallized TOPCon layers.

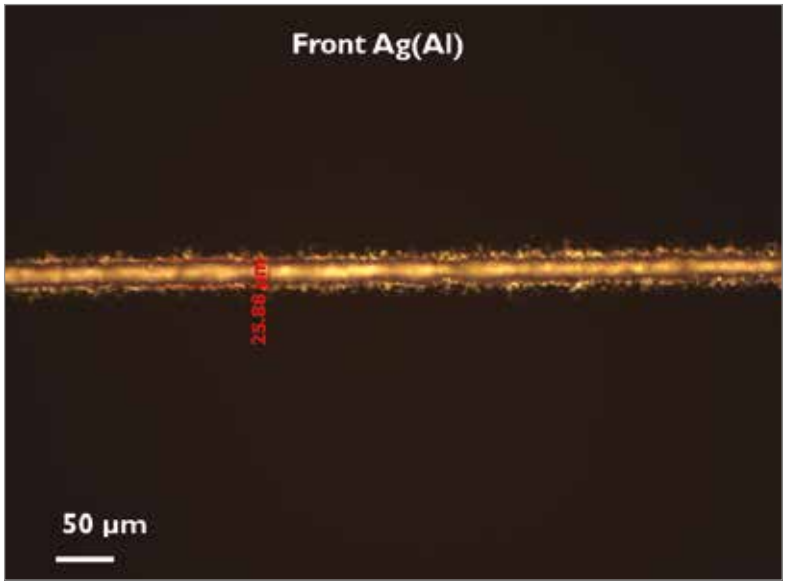
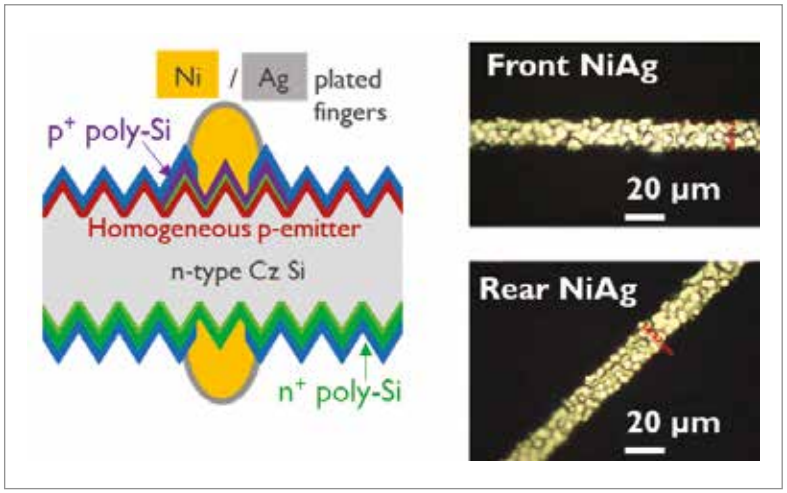


Figure 7. Example of fine-line screen printing at imec using commercially available screen-printing equipment and Ag(Al) paste to contact the p^+ emitter.



Source: Singh et al. [68]

Figure 8. Schematic of an n-PERT cell with blanket n^+ poly-Si at the rear, selective p^+ poly-Si at the front and plated NiAg fingers on both sides.

and SHJ, which consume more Ag per cell since Ag is printed on both sides, are gaining market share. That is why it is critical to rapidly reduce the Ag consumption per cell in those concepts compared with the 2020 median values of 150mg/cell (TOPCon) and 200mg/cell (SHJ) given in the ITRPV [10].

A first approach to reducing Ag consumption per cell is to print narrower fingers and implement multi-busbar interconnection technologies. Excellent progress with industrially available screen-printing equipment, standard mesh screens and commercially available Ag pastes has been achieved at imec in recent years [63]. This is now leading to ~25µm fingers, as shown in Fig. 7, and Ag consumption of around 50mg per side (M2 format) for TOPCon cells made at imec. Similar progress has also been reported by other companies [5,8] and R&D institutes such as Fraunhofer ISE using conventional screen printing [64] or parallel dispensing technology [65]. However, despite the excellent progress made in the last few years it will be difficult to reduce Ag consumption per cell to below 30mg per side (M2 format) without adopting busbarless interconnection technology, such as Smart Wire Contacting Technology (SWCT) currently employed with SHJ cells [66].

A second approach to significantly reducing Ag consumption per cell is to implement plated contacts. At imec, an innovative and simple, contactless, co-plating method has been developed with very low Ag usage per cell, since it relies on plating nickel (Ni) and a thin Ag capping layer [67]. This approach was recently adapted for n-PERT cells with poly-Si contacts implemented on both sides (see Fig. 8), to further reduce contact recombination losses; initial results obtained on test wafers were promising [68]. Not long ago, excellent progress was also reported using sequential nickel/copper/silver (Ni/Cu/Ag) plating in bifacial n-PERT cells with n^+ poly-Si at the rear side; efficiencies of up to 22%, limited by front-side recombination losses, were achieved [69]. With further developments, both the Ni/Ag and Ni/Cu/Ag plating approaches should be capable of reaching efficiencies above 24% and Ag consumption less than 10mg/cell; this would lead to Ag levels below 1.7g/W, representing a tenfold reduction with respect to the reported industry median in 2020.

"n-PERT cells with poly-Si passivating contacts are an attractive technology for pushing average module efficiencies above 22% in the coming years."

Conclusions

Given that the progress in p-PERC cell efficiency is expected to be more tedious and that major improvements in module design are already being implemented, n-PERT cells with poly-Si passivating contacts are an attractive technology for pushing average module efficiencies above 22% in the coming years. This paper has provided a short overview of historical developments that led to average efficiencies of above 24% being recently demonstrated in mass production. The main approaches in mass production today were presented, together with potential process simplifications. Finally, a key challenge for the future was discussed, namely the reduction of Ag consumption per cell.

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About EnergyVille

EnergyVille is a collaboration between the Belgian research partners KU Leuven, VITO, imec and Hasselt University in the fields of sustainable energy and intelligent energy systems. EnergyVille develops technology and knowledge to support public and private stakeholders in the transition to an energy-efficient, decarbonized and sustainable urban environment.

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