Photovoltaics International

THE TECHNOLOGY RESOURCE FOR PV PROFESSIONALS

Edition 46

Industry 4.0
How can digitisation and automation benefit solar manufacturing?

Sustainable manufacturing
Fraunhofer ISE details the solutions available to reduce carbon emissions from PV manufacturing

IBC technology
ISC Konstanz reveals how close the industry is to low-cost IBC cells with efficiencies greater than 25%

Heterojunction cell strength
As cells become ever-thinner, Hevel explores the trade-off between thickness and production losses

Shingle cells
CEA-INES details its recent work in shingle cell integration

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Foreword

Welcome to Photovoltaics International 46. The last year has been a period of profound change with the COVID-19 pandemic and subsequent response having deep and far-reaching consequences. The global effort to 'Build Back Better', with most countries dedicating significant resource to establishing greener economies, has been encouraging, and solar PV continues to be at the technological forefront of this paradigm shift.

Solar PV is itself on the cusp of a technological evolution. Recent analysis by PV Tech Research, the market research division of PVI publisher Solar Media, concluded that n-type cell technologies will dominate industry spending from 2024 onwards, indicating a dramatic shift away from p-type substrates. We explore some of these technologies in PVI 46, including within a paper from IMEC which explores the past, present and future of n-type passivated emitter and rear totally diffused (PERT) cells.

Of course, the technology itself is just one area of the wider manufacturing sector that is maturing. A paper from ISC Konstanz details the incorporation of 'Industry 4.0' – the adoption of automated and digitised industrial practices – into the solar manufacturing value chain, determining which approaches can be used to quickly and easily accelerate product ramps, while also exploring the concept of a scalable and modular system compatible with any hardware.

Meanwhile, the European Commission continues to offer support for a solar manufacturing renaissance on the continent, highlighting the sector as a cornerstone of its post-pandemic economic strategy. The plans are the subject of much debate in the industry, and the prospective inclusion of a carbon emissions limit on solar products to be used by member states could be a crucial driver.

The Fraunhofer Institute for Solar Energy Systems writes on the sustainable manufacturing solutions that can help drastically reduce carbon emissions associated with the production of solar modules. As you can read, Fraunhofer ISE's analysis shows that utilising less energy-intensive seed manipulation for artificially controlled defect techniques can produce a climate change impact of just 21.36g of CO_2 equivalent per kilowatt hour, as opposed to 43.32g CO_2-eq/kWh recorded from a CZ PERC system in China.

In short, the pages of PVI 46 illustrate an industry which is becoming more technologically advanced, more efficient and cleaner simultaneously, already laying the foundations for the critical next phase of growth.

Thank you for reading, and we hope you enjoy the journal.

Liam Stoker
Editor in chief
Solar Media Ltd.

Editorial Advisory Board

Photovoltaics International's primary focus is on assessing existing and new technologies for "real-world" supply chain solutions. The aim is to help engineers, managers and investors to understand the potential of equipment, materials, processes and services that can help the PV industry achieve grid parity. The Photovoltaics International advisory board has been selected to help guide the editorial direction of the technical journal so that it remains relevant to manufacturers and utility-grade installers of photovoltaic technology. The advisory board is made up of leading personnel currently working first-hand in the PV industry.

Our editorial advisory board is made up of senior engineers from PV manufacturers worldwide. Meet some of our board members below:

Prof Armin Aberle, CEO, Solar Energy Research Institute of Singapore (SERIS), National University of Singapore (NUS)

Prof Aberle's research focus is on photovoltaic materials, devices and modules. In the 1990s he established the Silicon Photovoltaics Department at the Institute for Solar Energy Research (ISFH) in Hamelin, Germany. He then worked for 10 years in Sydney, Australia as a professor of photovoltaics at the University of New South Wales (UNSW). In 2008 he joined NUS to establish SERIS (as Deputy CEO), with particular responsibility for the creation of a Silicon PV Department.

Dr. Markus Fischer, Director R&D Processes, Hanwha Q Cells

Dr. Fischer has more than 15 years' experience in the semiconductor and crystalline silicon photovoltaic industry. He joined Q Cells in 2007 after working in different engineering and management positions with Siemens, Infineon, Philips, and NXP. As Director R&D Processes he is responsible for the process and production equipment development of current and future c-Si solar cell concepts. Dr. Fischer received his Ph.D. in Electrical Engineering in 1997 from the University of Stuttgart. Since 2010 he has been a co-chairman of the SEMI International Technology Roadmap for Photovoltaic.

Dr. Thorsten Dullweber, Head of PV Department at the Institute for Solar Energy Research Hamelin (ISFH)

Dr. Thorsten Dullweber is leading the PV Department and the R&D Group Industrial Solar Cells at ISFH. His research work focuses on high efficiency industrial-type PERC and bifacial PERC+ silicon solar cells, where he co-authored more than 100 Journal and Conference publications. Before joining ISFH in 2009, Thorsten worked as project leader for DRAM memory chips at Infineon Technologies AG. He received his Ph. D. degree in 2002 for research on Cu(In,Ga)Se2 thin film solar cells. Thorsten is member of the Scientific Committees of the EU-PVSEC and SNEC conferences.

Dr. Wei Shan, Chief Scientist, JA Solar

Dr. Wei Shan has been with JA Solar since 2008 and is currently the Chief Scientist and head of R&D. With more than 30 years' experience in R&D in a wider variety of semiconductor material systems and devices, he has published over 150 peer-reviewed journal articles and prestigious conference papers, as well as six book chapters.

Florian Clement, Head of Group, MWT solar cells/printing technology, Fraunhofer ISE

Dr. Clement received his Ph.D in 2009 from the University of Freiburg. He studied physics at the Ludwigs-Maximilian-University of Munich and the University of Freiburg and obtained his diploma degree in 2005. His research is focused on the development, analysis and characterization of highly efficient, industrially feasible MWT solar cells with rear side passivation, so called HIP-MWT devices, and on new printing technologies for silicon solar cell processing.

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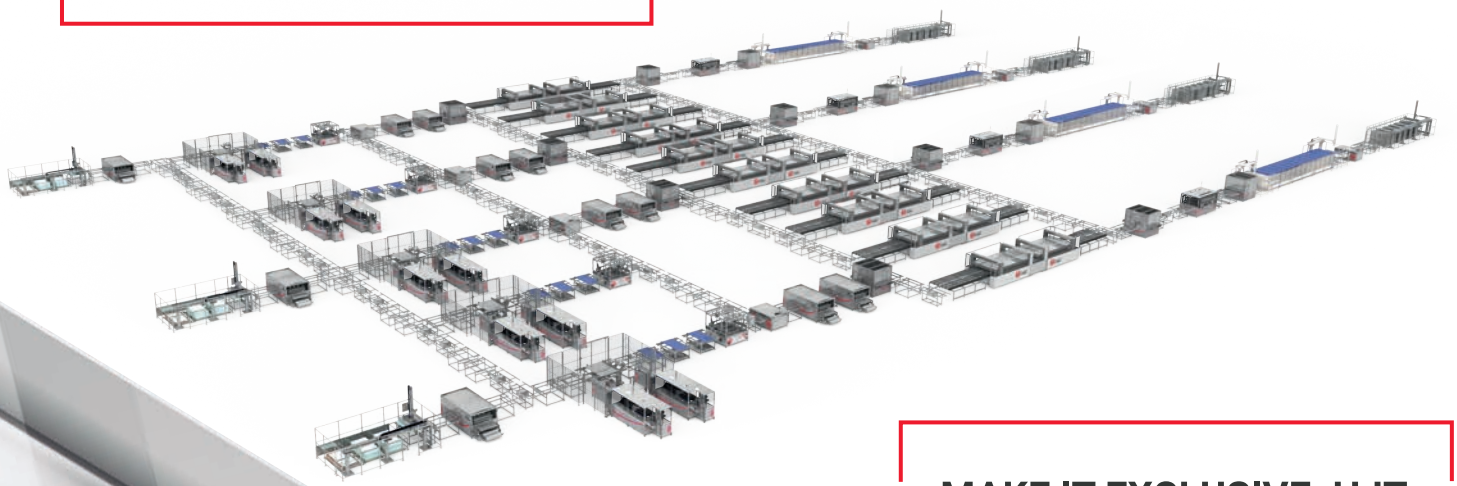

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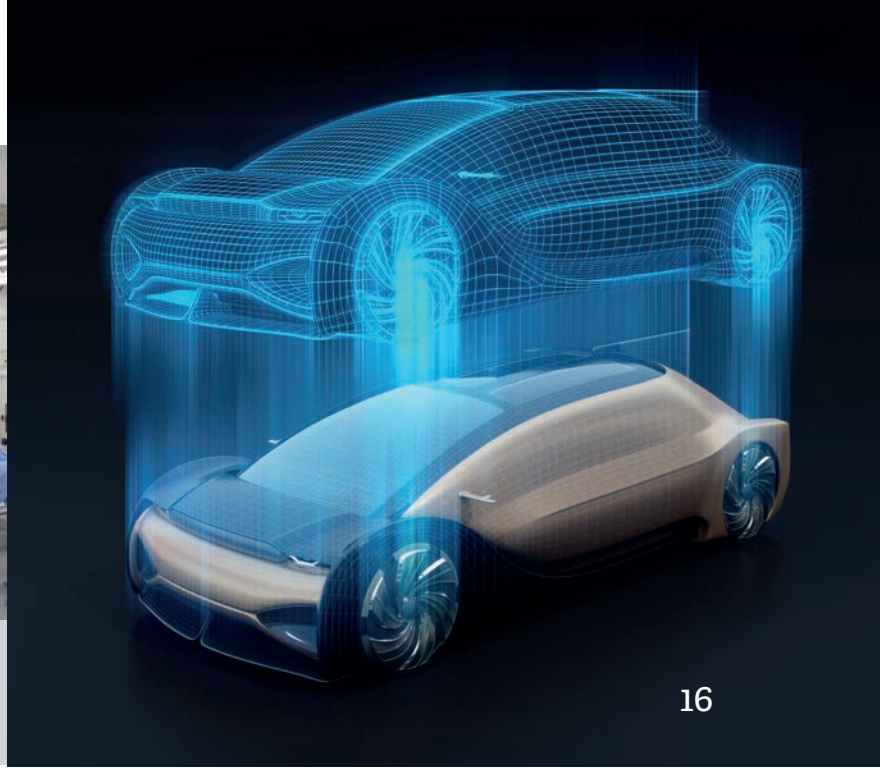

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PV MANUFACTURING & TECHNOLOGY QUARTERLY REPORT

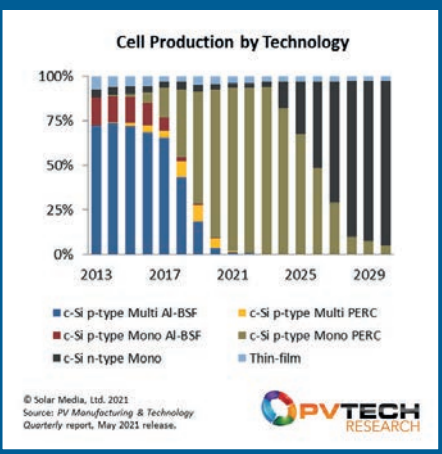
For the past five years, the PV Manufacturing & Technology Quarterly report has been the leading market research report to the PV industry, tracking bottom-up technology trends across the entire manufacturing value-chain, through to global module shipment analysis.

PVTECH RESEARCH

The report covers production metrics for the industry and the leading solar manufacturers across the entire value-chain, including polysilicon, ingot, wafer, cell, and c-Si & thin-film modules:

- Over 100 companies are analysed bottom-up
- Module shipments are identified by quarter for each module supplier
- Forecasts for new capacity, technology upgrades and expansions
- Capex and R&D spending for all manufacturers

With the shift to p-mono PERC complete the report now looks ahead to the n-type shift and the companies driving change in the short-term with accurate tracking of the cell producers and n-type architectures currently setting the scene for the pending technology change in 3-5 years from now.



Our current forecast is pointing at 2024 being the key year for n-type, with this year – and most of 2022-2023 – setting the stage for what will follow. The graphic above shows this forecast, where p-mono PERC market-share can be viewed largely as the transition phase between p-multi and n-mono.

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PV-Tech's Market Research division provides the industry with accurate and timely data to allow PV manufacturers, and equipment and material suppliers, to understand existing and future technology landscapes and roadmaps.

Sustainable PV manufacturing solutions for relaunching the European PV manufacturing industry

Peter Brailovsky, Lorenz Friedrich, Sebastian Nold, Stephan Riepe & Jochen Rentsch, Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, Germany

Abstract

To embrace the terawatt-scale challenge of the PV market growth, a low-carbon and resource-efficient pathway has to be guaranteed. An approach for doing this is to enable market mechanisms that account for the greenhouse gases emissions, and their associated costs, from PV systems and components. Under such conditions, it is expected that different technological options and solutions will have to be considered for the development and deployment of PV power plants and systems. In this paper, the economic competitiveness and environmental performance of the production of PV systems in Europe and China are assessed. Results are presented for the currently dominant recharged Czochralski (Cz) wafer technology, and for the less energy-intensive seed manipulation for artificially controlled defect technique (SMART) cast-mono (CM) technology. The analysis shows that SMART technology can be used to produce mono PERC systems with a climate change impact of just 21.63g CO2-eq/kWh, while a Cz PERC system produced in China will entail an emission of 43.32g CO2-eq/kWh. Around 45% of this reduction is achieved by having the production located in Europe. SMART technology yields a reduction potential of 9% of the associated global warming potential (GWP), when compared with the more energy-intensive Cz growth technology. Both Cz and SMART technologies can be produced at a competitive cost in Europe when carbon-associated costs are taken into consideration, leading to total costs of ownership of 21.5 and 21.6€ct/Wp respectively.

Motivation

The PV market is expected to grow from about 740GW total installed capacity worldwide in 2020 to about 2,840GW in 2030 [1]. For this deployment it is assumed that the market share of mono-Si wafer-based PV will remain at around 95%, which represents a demand of approximately 2,000GW of PV capacity over the next 10 years. The associated environmental impacts of this development with respect to emissions of greenhouse gases and total energy consumption, along with other impacts on the biosphere and on human health, must be considered in order to follow a sustainable development path. This is especially true for energy-intensive processes in the PV value chain, such as the production of polysilicon, the crystal growth process of silicon and the production of balance-of-system (BoS) components.

"It is essential that the growth of the PV market is achieved as cleanly as possible and that resources are used with an ever-increasing efficiency."

According to the principles of the European Green Deal [2], it is essential that the growth of the PV market is achieved as cleanly as possible and that resources are used with an ever-increasing efficiency. Adhering to these principles, along with satisfying the economic competitiveness, represents both a challenge and an opportunity for the relaunch of the European PV manufacturing industry.

Major Tier 1 PV producers – such as Jinko Solar, First Solar and LONGi – have already made public statements with regard to sourcing 100% renewable electricity for their global operations between the years 2025 and 2028 [3]. This positive news shows how relevant a product sustainability strategy has become to market-leading companies, but clearly this strategy faces its own implementation and operational costs. The establishment of a sound compliance system and chain of custody along the companies' value chains is challenging and may prove difficult if the scope of their commitments includes the production of the energy-intensive aluminium frames, glasses and BoS components. It is also challenging to demonstrate that these efforts generate net greenhouse gas emission savings for the economy and not just a virtual effect where other products and consumers are fed with a slightly more carbon-intensive electricity than before. Additionally, the environmental hazard potentials of raw materials extraction and production should also be addressed by the industry with the same priority that is given to carbon footprints [4].

In this paper the cost competitiveness and environmental performance of the production of PV systems and their components in the European Union and China are assessed. Results are presented for the currently dominant recharged Czochralski (Cz) wafer technology and for the less energy-intensive SMART (seed manipulation for artificially controlled defect technique) cast-mono (CM) wafer technology. Both wafer types are processed into passivated emitter and rear contact (PERC) solar cells, as these are the mainstream solar cell product. Modules with half-cut PERC cells and multi-busbar interconnection technology are then considered.

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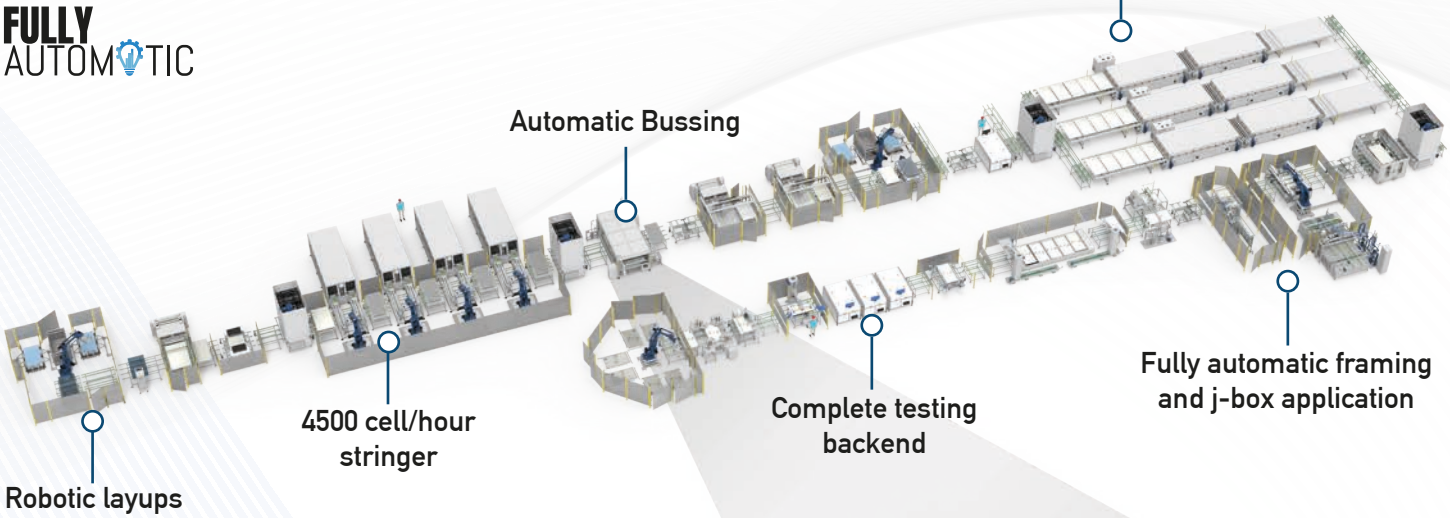

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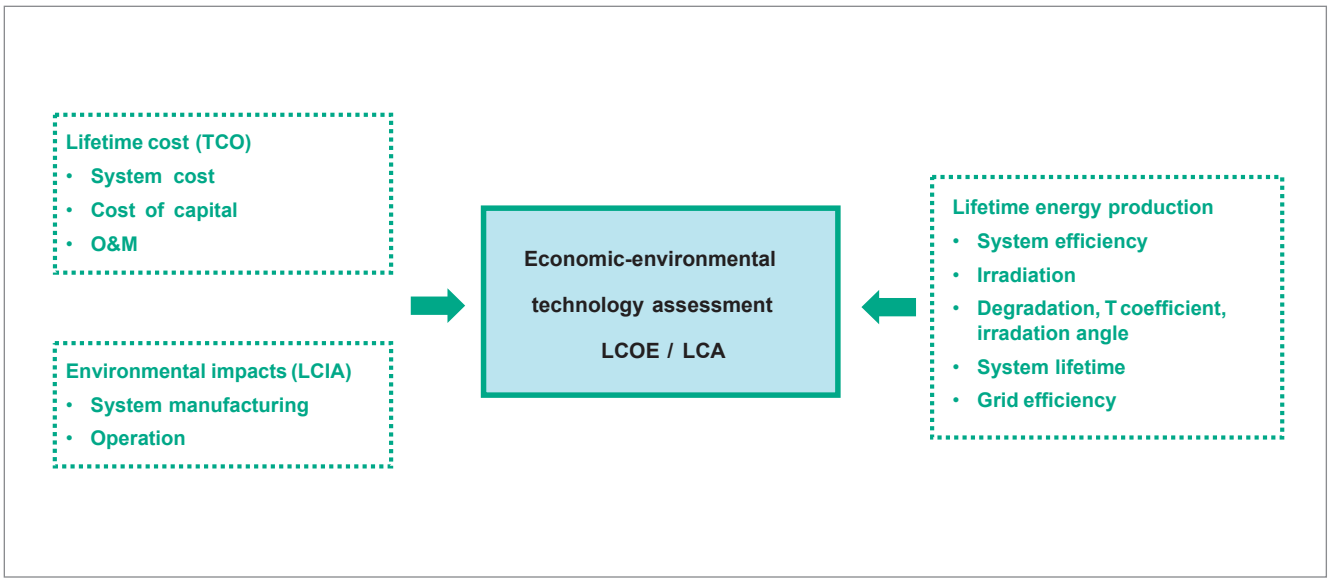

Figure 1. Structure of the technology assessment based on life cycle assessment (LCA) and total cost of ownership (TCO).

Approach

For new technologies, a technology assessment based on total cost of ownership (TCO) is not sufficient, since the cost uncertainty often dominates the cost advantage between technology options. Moreover, a singular view on the environmental impacts has limited predictive power for rational technology decisions. What is obvious is that an environmentally friendly module cannot achieve a significant market share without economic competitiveness.

Fig. 1 shows the general structure of the integrated assessment. The approach follows Norris' proposals for integrating full life cycle costing (LCC) and full life cycle assessment (LCA) [5].

An LCA was carried out using Umberto LCA+ version 10.0 software and the Ecoinvent version 3.6 database. In compliance with the ISO standards 14040/4 for the general LCA procedure, in this assessment the IEA PVPS guidelines on LCA for PV and the European Product Environmental Footprint Category Rules for PV were considered [6–8].

The goal of this analysis is to assess 1) the environmental impacts of PV electricity with selected impact categories, 2) the corresponding levelized cost of electricity, and 3) the effects of carbon pricing at selected production locations in China and the European Union. The selection of the impact categories is carried out according to the status of available and modelled production data of a PERC module production process.

The LCA part of this study is an attributional assessment; in other words, no recycling bonus/waste treatment process of the PV modules and BoS components is included. The functional units are 1Wp of module power, rated under standard test conditions (STC) and 1kWh of electricity generated by the PV system.

The scope of assessing two different crystallization and cell concepts, and the corresponding production processes, includes mg-Si and poly-Si, and wafer, cell and module production (see Fig. 2). The data for BoS components (excluding inverter) and background processes are derived from the Ecoinvent 3.6 database. It is assumed that the whole PV system, including BoS components, is manufactured in a single production location, namely either China or the EU. Therefore, transportation is modelled for the whole PV system from the production site to the location where the PV system is installed. As the focus is on final PV installations in Europe, the cost of shipping modules from China to Europe is therefore included.

To derive the inputs used in the life cycle assessment and cost-of-ownership economic assessment, the SCost model of Nold et al. (2012) is used. The core of SCost is a detailed bottom-up model of the whole PV value chain based on the widespread SEMI standard composed of several layers to accurately represent production activities, process steps, and wafer, cell and module production processes [9,10].

The cast-mono technology data used in this work are based both on experimental data for the growth of CM-Si via the SMART seeding approach [11] and on industry information about equipment and process parameters. In order to study the potential of CM-Si technology for the next decade, data from state-of-the-art G8 furnace concepts (SCU 1500, ALD Vacuum Technologies) were used for the analysis. For the material quality distribution, data from growth experiments

"An environmentally friendly module cannot achieve a significant market share without economic competitiveness."

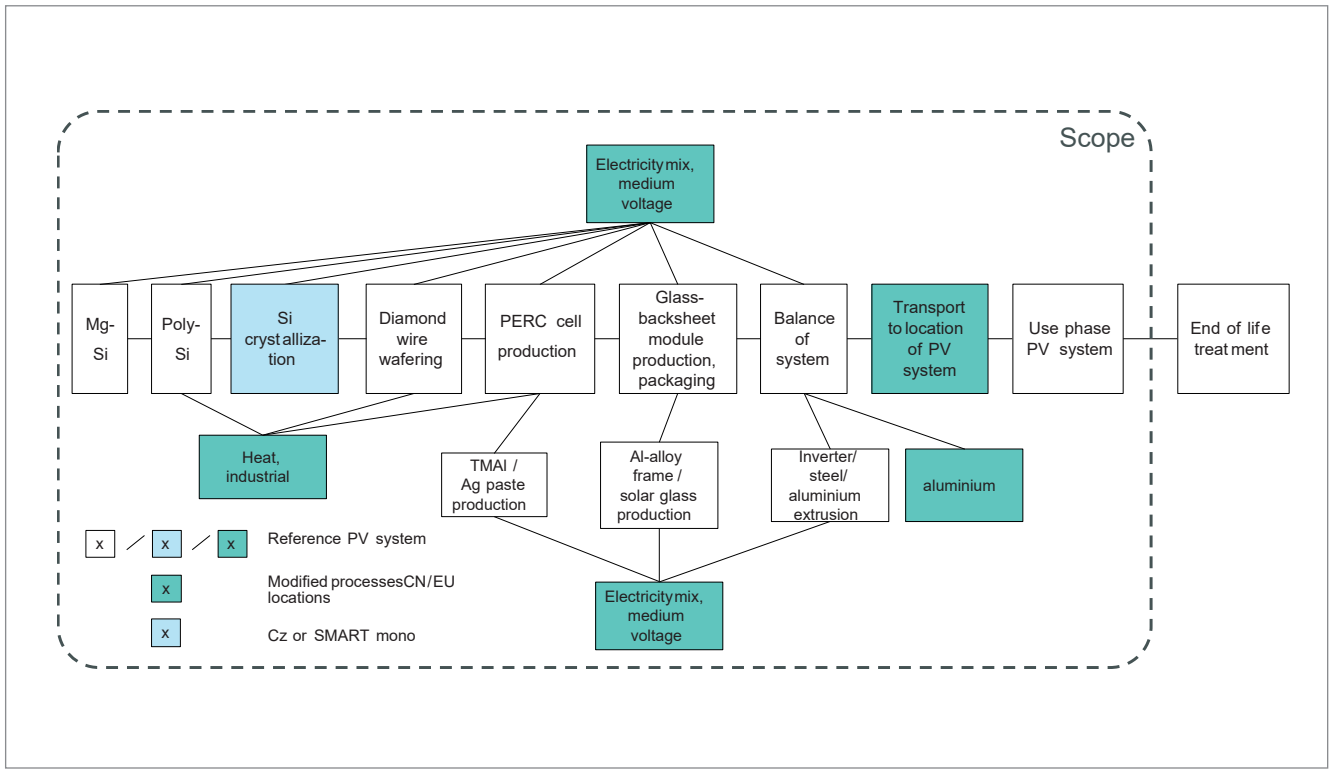

Figure 2. Scope of regional assessment. The modifications to the processes indicated in green enable a regional assessment of the environmental impacts of PV systems produced in Europe (EU, RER) and China (CN).

Parameter	Value
Feedstock charge [kg]	1,500
Seed height [mm]	20
Ingot side length [mm]	1,420
Brick side length [mm]	166
Number of bricks	64
Growth velocity [mm/h]	12

Table 1. Input data for CM-Si growth process (M6 wafer size).

Parameter	Value
Feedstock charge [kg]	360
Ingot height [m]	4
Ingot diameter [mm]	226
Pulling speed [mm/min]	1.7

Table 2. Input data for Cz-Si growth process (M6 wafer size).

utilizing laboratory processes with G2-sized ingots, equivalent to 75kg of Si feedstock, and G6-sized industrial processes, with 650kg of Si feedstock and SMART seeding concept, were evaluated. On the basis of these results, the main assumptions for material quality distribution, and thus potential yield, were derived for a G8 system with crucible sizes adapted to an optimal ingot side length for M6 wafer production. An overall electricity consumption of 6.8kWh/kg of crystallized silicon is assumed [12].

Additional input values for the CM-Si process model are shown in Table 1.

A general width of 30mm for ingot side cuts and a 1mm grinding loss per brick were accounted for. After cropping the top and bottom of the brick including the seed, a maximum usable brick height of 85% of total ingot height was calculated for all bricks. The brick yield – defined as the brick mass that meets the required material quality after squaring and polishing – strongly depends on the quality assumptions of the investigated growth process and the material requirements of the subsequent cell process. In order to model a more realistic yield for CM-Si material that meets the quality requirements for further cell production, a usability of 70% of the outer brick material and 80% of the inner was calculated, resulting in overall brick yield values of 53.1% for the M6 process.

For the Cz-Si growth model, the input data are based on an industrial Cz furnace including a recharging unit, a 36" crucible and a receiving chamber of more than 4m in height and an average of 4.5 pulls of 4m-long ingots per crucible. An overall energy consumption of 30kWh/kg of crystallized silicon was assumed [12]. Additional input values for the Cz-Si process model are shown in Table 2.

A maximum ingot usability of 85% after the cutting of seed, shoulder and end cone is assumed for all ingots, without taking into account any remelting processes. The usable brick mass considering the geometric constraints of creating a square wafer from a round ingot was thus calculated to be 58.8% for the M6 format.

As regards the following steps, the input data were mostly the same for both CM-Si and Cz-Si wafers, with the exception of the cell efficiency, and subsequently the module power. A PERC solar cell process was assumed to have an average efficiency of 22.3% for the CM-Si material, compared with 22.5% for the Cz-Si. Prior to module manufacturing, all cells were cut into half cells for the M6 format. The modules were modelled as glass–backsheet modules with 120 half cells. The average module power for Cz-Si material was thus calculated to be 372Wp; in the case of CM-Si, this worked out to be 371Wp for analogue modules. A summary of all relevant parameters is given in Table 3.

The modules are combined with the necessary electronic and roof-mounting equipment to form a residential rooftop PV system with a rated power of 15kWp at an average European location. An average annual global tilted irradiation of 1,331kWh/m² and a degradation of 0.7% are considered for a system lifetime of 30 years.

Cell type	Cz	SMART mono
Ingot/wafer		
Wafer area (M6) [cm²]	274.2	275.6
Wafer thickness [µm]	170	
Kerf loss (wafer slicing) [µm]	80	
Cell		
Cell area (half cell) [cm²]	137.1	137.8
Cell efficiency (STC) [%]	22.50	22.30
Module		
Module area [m²]	1.85	
Half cells per module	120	
Module efficiency [%]	20.11	20.04
Module power [Wp]	372.3	370.9

Table 3. Performance parameters for the selected technologies.

Carbon footprint

The resulting carbon footprint of the production of PV systems and their components was significantly smaller in the EU than in China (see details in Fig. 3); this holds true for both Cz and SMART cast-mono PERC technologies. The main driver for this smaller carbon footprint lies in the electricity grid mix which powers the chemical vapour deposition (CVD) Siemens bell reactors for poly-Si production, the ingot pullers for Cz-Si crystallization, and the production of inverter components, electrical installation, and aluminium and steel mounting structures. SMART technology provides a smaller carbon footprint than with Cz for both regions.

The GWP results for PV electricity (Fig. 4) range from 21.63g CO_2-eq/kWh for the SMART mono PERC system produced in the EU to 43.32g CO_2-eq/kWh for the Cz PERC system produced in China. The GWP advantage of SMART crystallization is a potential reduction of around 9% compared with the established Cz technology for the EU and China regions. Another 45% GWP reduction can be realized by producing the PV systems in the EU instead of China.

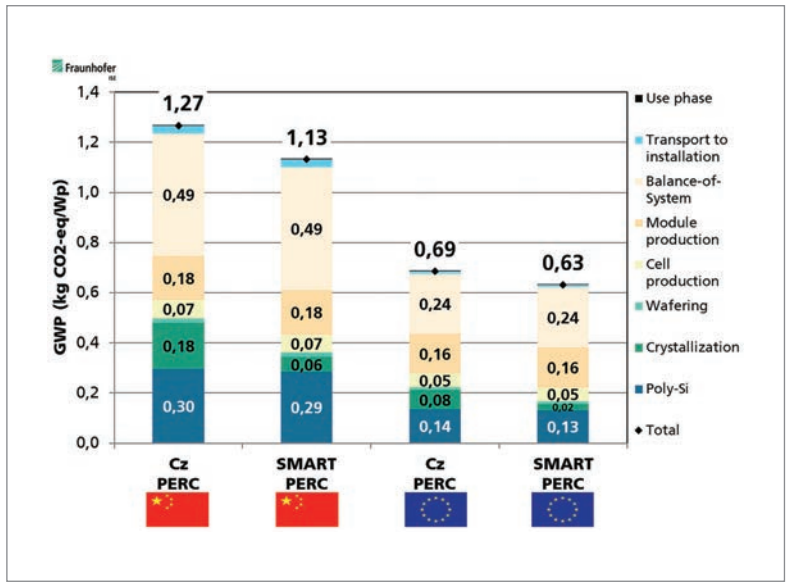

Figure 3. Global warming potential (GWP) of 15kWp Cz and SMART mono PERC systems, produced in CN and the EU, and installed on a rooftop in an average European location. GWP is calculated with IPCC 2013, 100 years.

Effects of a carbon pricing

Up to now, there have been at least 45 countries worldwide that have implemented a national carbon tax and/or an emissions trading system (ETS) initiative [13]. European countries were the first to establish such practices, and now the EU commission is discussing the introduction of a broad border carbon tax for the whole region [14].

As the EU's PV industry cost structure and prices already take into consideration carbon allowances, the introduction of a border carbon tax is expected to have a maximum effect on imported goods from China. In Fig. 5 the effect of a varying carbon price on the differential CO_2-eq costs of a PV module is shown for both cases – a Cz system as well as a SMART mono PERC system.

A border carbon tax introduced by the EU will certainly help as a ground leveller for local PV manufacturers. Goods produced by energy-intensive industries in the EU have already been facing 'carbon taxes' since 2005 by the cap-and-trade EU emissions trading system (EU ETS) [15], where they need to acquire emission allowances

"The GWP advantage of SMART crystallization is a potential reduction of around 9% compared with the established Cz technology for the EU and China regions."

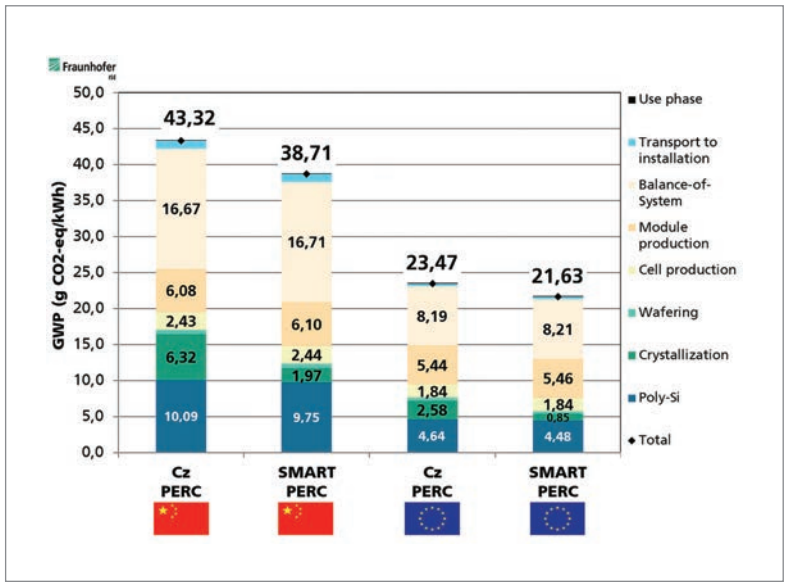

Figure 4. Global warming potential (GWP) of PV electricity generated by 15kWp Cz and SMART mono PERC systems, produced in CN and the EU, and installed on a rooftop in an average European location with a 30-year lifetime and 29.25MWp lifetime electricity generation. GWP is calculated with IPCC 2013, 100 years.

"The introduction of a border carbon tax is expected to have a maximum effect on imported goods from China."

for a current market price of ~€34/kg[3] CO_2-eq [16,17] (which will increase in future years). On the other hand, goods imported into the EU enjoy the luxury of being sold without assuming any carbon levy if this has not already been imposed by the country of origin of the goods and components production.

As China is already in the process of establishing a national ETS [18], a compensation system between the EU and China will have to be designed in the near future.

TCO assessment

The TCO results presented account for all fixed, operational, maintenance and yield loss costs over the life of the range of equipment needed to produce the PV systems and their components for the selected regions. As can be seen in Fig. 6, the net costs of modules from China, including shipping costs to Europe, are lower than the costs of those from the EU by ~1.9€ct/Wp, for both Cz and SMART. The competitive advantages behind this are to be found in the economies of scale for consumables, electricity prices, labour costs and non-carbon-related levies. Wider differences are found in the wafer and module production step costs. The costs of PV modules with SMART technology are slightly higher than the ones with Cz; this is explained by a net increase in costs due to labour costs versus electricity saving costs.

If we now consider and implement a carbon border tax for PV modules imported into Europe similar to the already existing EU emission trading system, and assume a future carbon price of around €100/10[3]kg, the differential costs of these two taxes need to be paid on top for the Chinese modules. In reality, the carbon border tax needs to be paid for the full carbon-equivalent emissions of the Chinese module and the full carbon-equivalent emissions of the European module.

The corresponding additional cost of PV modules will increase the net production costs of

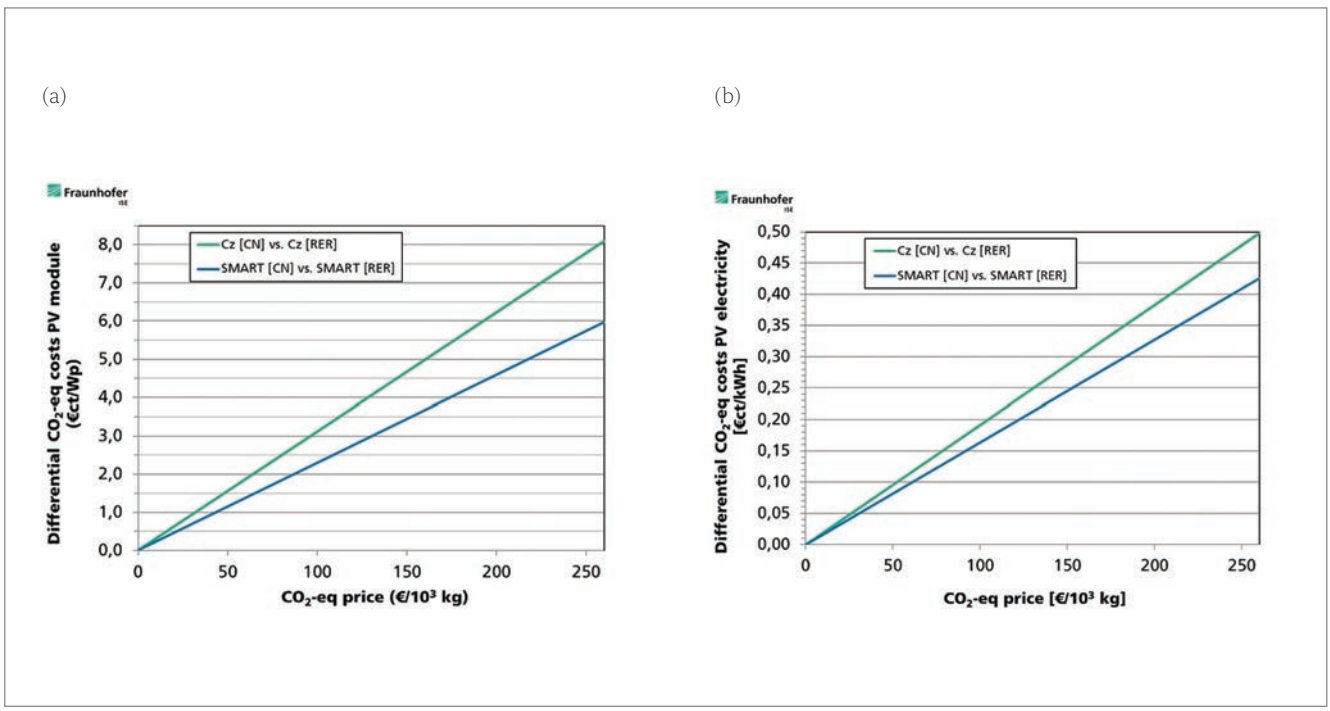

Figure 5. Cost difference of (a) PV modules and (b) PV electricity generated by PV systems produced in CN and the EU (RER) and installed in an average European location, taking a carbon pricing of the EU into account.

Cz PERC and SMART PERC modules from China by 15% and 11%, respectively, and will certainly level the competitive playing field for European producers (see Fig. 7).

Conclusion and outlook

The enormous PV market growth expected for the next decade will consume high amounts of raw materials and energy in the production process. It is therefore preferable to achieve this growth with an environmental impact and energy consumption as low as possible in order to achieve a rapid decarbonization of the energy sector in accordance with the Paris Climate Agreement.

The main driver for a smaller carbon footprint lies in the electricity grid mix, especially within the energy-intensive production steps such as poly-Si and ingot manufacturing. The environmental advantage of producing a PV system in Europe is highlighted by a 45% GWP reduction compared with a PV system made in China.

Furthermore, with the right technology choice, the carbon footprint of the production chain can even be improved by using SMART cast-mono silicon wafers in comparison to Cz silicon wafers for the production of PERC solar cells. With SMART crystallization, an additional GWP benefit of a potential reduction of around 9% compared with the established Cz technology for both the EU and China regions can be realized.

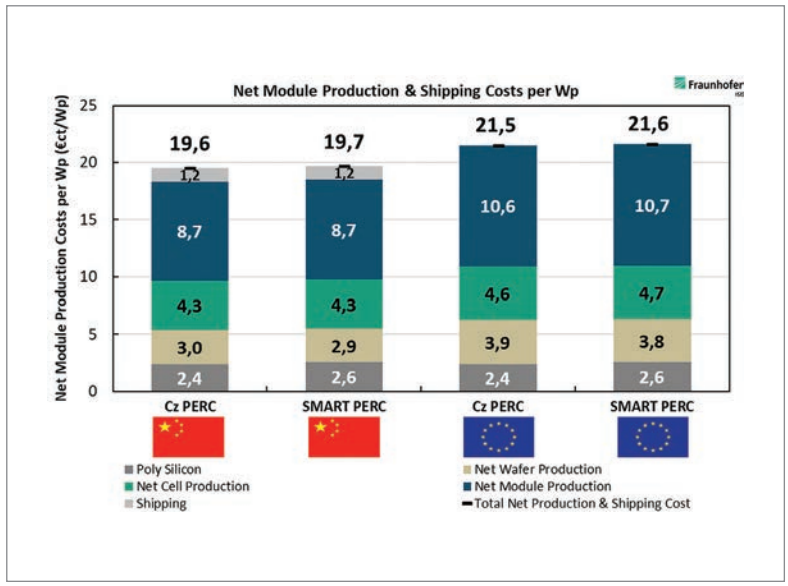

Figure 6. Net module production costs for Cz and SMART mono PERC PV modules produced in CN and the EU. Shipping costs from China to Europe for the whole module are 1.2€ct/Wp. Production processes are modelled bottom up for a total production capacity of 5GW and assessed using a total-cost-of-ownership (TCO) approach. Polysilicon costs are modelled with an average world market price of €10/kg.

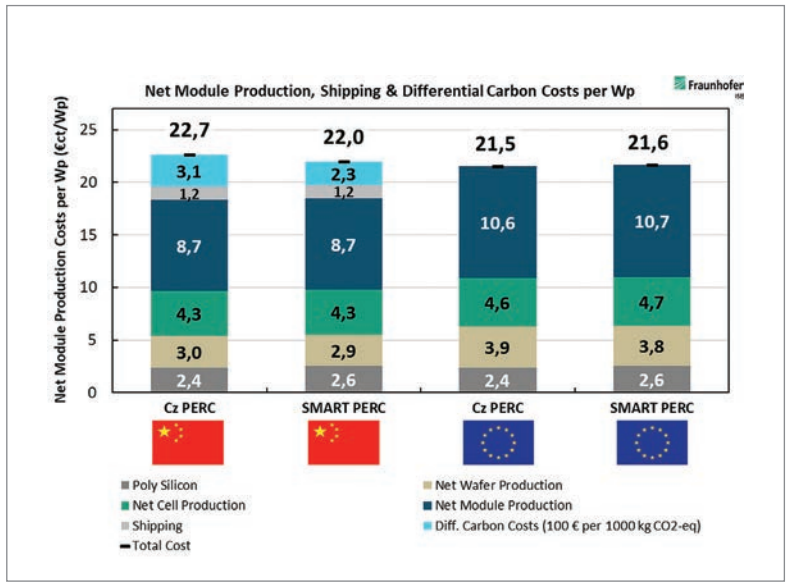

Figure 7. Net module production costs for Cz and SMART mono PERC PV modules produced in CN and the EU, including a differential carbon cost for a future carbon price of €100/10^{3}kg.

"The environmental advantage of producing a PV system in Europe is highlighted by a 45% GWP reduction compared with a PV system made in China."

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Pragmatic organic integration of Industry 4.0 in the PV industry

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Abstract

Industry 4.0 has often been discussed and investigated in relation to its benefits for the PV industry. Many solutions require the set-up of a complex complete system for the entire manufacturing process and possibly even for the raw materials. Particularly for existing manufacturing operations or for ramp-up, such complex solutions are often out of the question. The aim, therefore, is to discuss in this paper what approaches from the digitalization field can be used quickly and easily to accelerate ramp-up, to analyse overlapping data and to improve production either manually or automatically. The concept of a scalable, strictly modular system that works with any hardware and leaves the choice of application to the user is presented. All data will reside in a database, from which they can be retrieved with, for example, Excel, jmp or other statistical/monitoring or management software. In addition, standards for wafer tracking are proposed, and a way of integration with current digital twin standards is suggested so that the system can be easily extended. The concepts described are part of a FlexFab system: RCT and ISC are working together on a factory concept in which different cell and module designs (here, bifacial n-type back-contact ZEBRA and PERC) can be manufactured in parallel. In the production process, it is possible to continuously vary the proportion of different cells as required.

Introduction

How does digitalization and Industry 4.0 benefit PV? An organic way of realizing a meaningful digitized PV factory will be discussed, where equipment, measuring devices and environmental sensors are equipped with digital twins or minimal digital twins. These virtual representations communicate autonomously using open standards that are recognized throughout industry. The data can be accessed with almost any software. 'Minimal' means that only the necessary data are collected and can be easily expanded.

Benefits for ramp-up

The ramp-up process is arguably the most complex operation that any PV factory will ever experience. Each individual plant presents its own start-up difficulties: facilities such as ventilation, clean water and automation will have just been set up and will therefore be more prone to errors than after operating continuously for some time. Operators also need to be trained and may make frequent mistakes until they are fully qualified. In the light of these conditions, the complex equilibrium of a stable – and, as far as possible, efficiency-optimized – manufacturing process for solar cells needs to be reached during ramp-up and the system broken in.

"Ramp-up generally still takes place manually in many factories."

Despite the drawbacks, ramp-up generally still takes place manually in many factories: the settings of individual systems and the measurement results, such as sheet resistance, finger width and *I–V* parameters, are noted down and transferred to Excel tables or read out from the individual systems. Engineers then laboriously analyse the dependencies of individual process steps and environmental influences.

As an example, in one project large fluctuations in cell voltage and efficiency were observed; the cause of this was not readily apparent at first, until a technician noticed that the results always improved after a rainfall. It transpired that filters in the ventilation system were defective, allowing metal particles to enter the clean room (Figs. 1 and 2). However, when the rain had cleaned the outside air, the air in the clean room was also clean and the results were significantly better.

The efforts to find the source of the problem were enormous: all the data had to be collected, and many other hypotheses tested and discarded before the problem was eventually solved. It would have clearly been a huge help had all the data already been made available automatically at the start of ramp-up, such as measurement results, device parameters and also seemingly aberrant environmental data. If, in addition, statistical methods had been used to automatically check for correlations, the issue would probably have been detected much earlier.

Of course, steps like those described above can be carried out using a manufacturing execution system (MES) – provided such a system has been commissioned and is already fully functional before ramp-up begins. Alternatively, each individual plant, each measuring device and each sensor could be equipped with a digital interface right at the point of commissioning, and a 'minimal digital twin' created, which would allow each device to be queried uniformly. The data can be written into databases or directly used by programs of the customer's choosing, for example Excel or statistical analysis programs. In this way, the application is isolated from the data provision.

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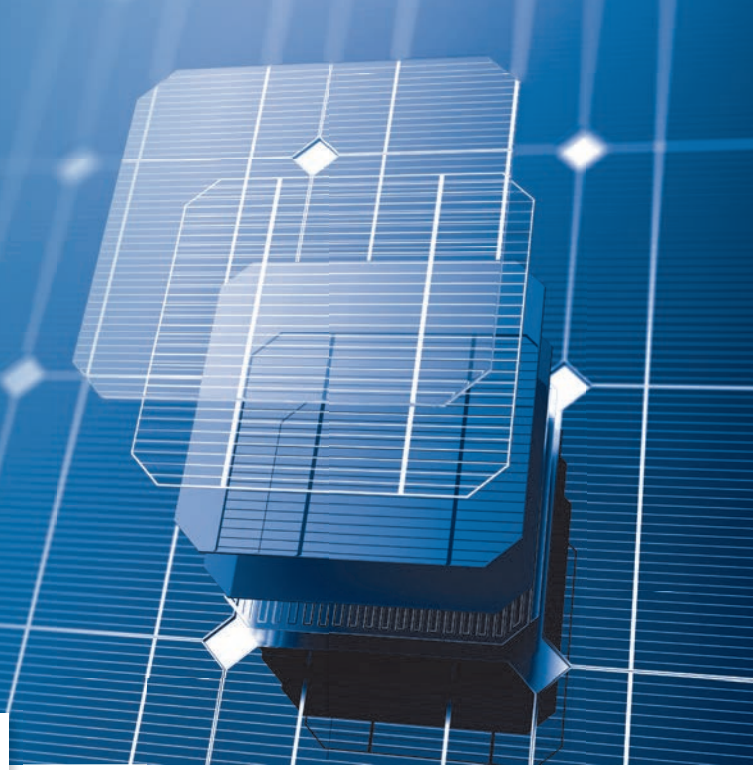

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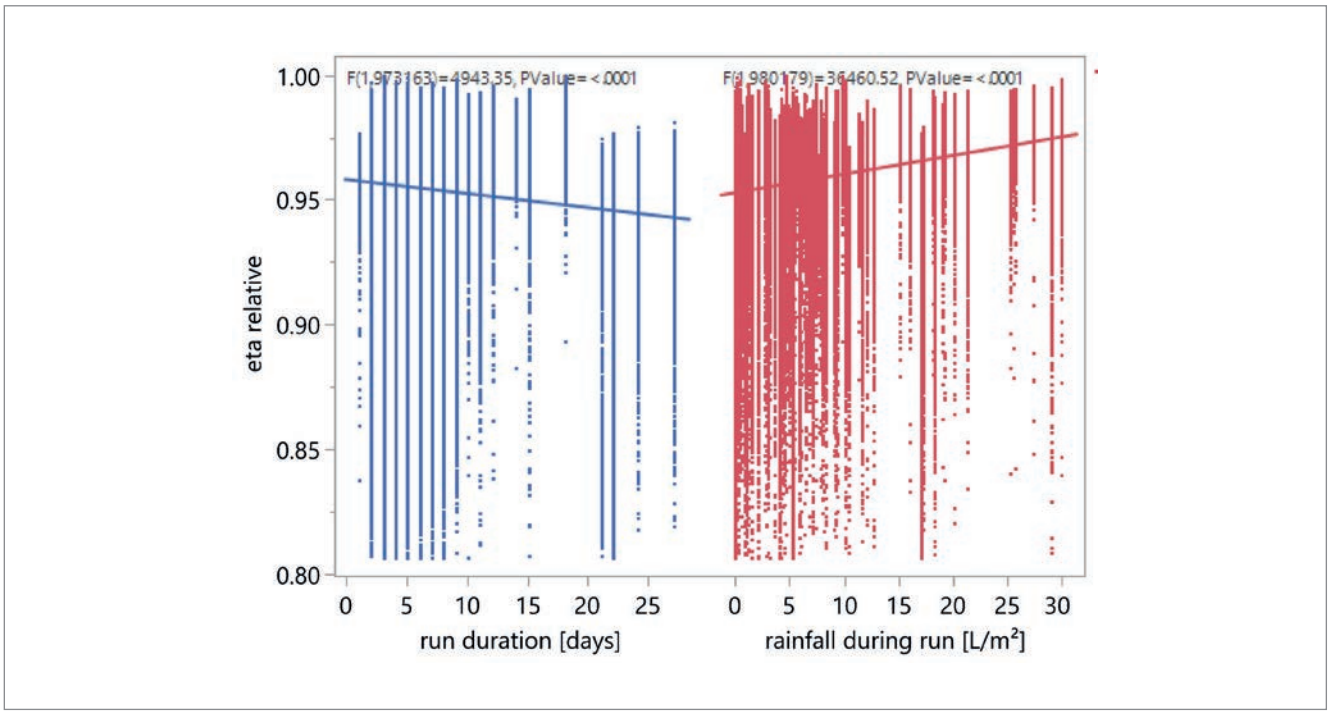


Figure 1. Strong dependency of efficiency on rainfall in a ramp-up project. It was found that a defective filter led to metal-containing dust in the clean room. After a rainfall, the outside air was clean and therefore no contaminated air entered the clean room.

Benefits for manufacturing reports

In an operational PV production set-up, different parts of the operation need different information. The *shift supervisor* must have a continuous and up-to-date overview of yield and the most important cell parameters; they must be able to see at least the current errors from the plants, and preferably even more parameters as needed. The *operator* needs to be informed about tasks. The *management* should be able to query yield, uptime and quality of the cells or modules at any time and for any period.

Each of the three levels of operation mentioned above may wish to use different software. Quality assurance requires the development of, for example, an Excel tool into which data are fed. The operator might use an in-house-developed app for their cell phone or smartwatch to automatically advise them to go to a specific plant at any time. The accounting department will probably want to integrate results directly into accounting software.

An MES, of course, can achieve this variety of software needs; however, this type of system involves complex, centralized software. Digital twins and the use of Industry 4.0 technologies would mean more

"In an operational PV production set-up, different parts of the operation need different information."

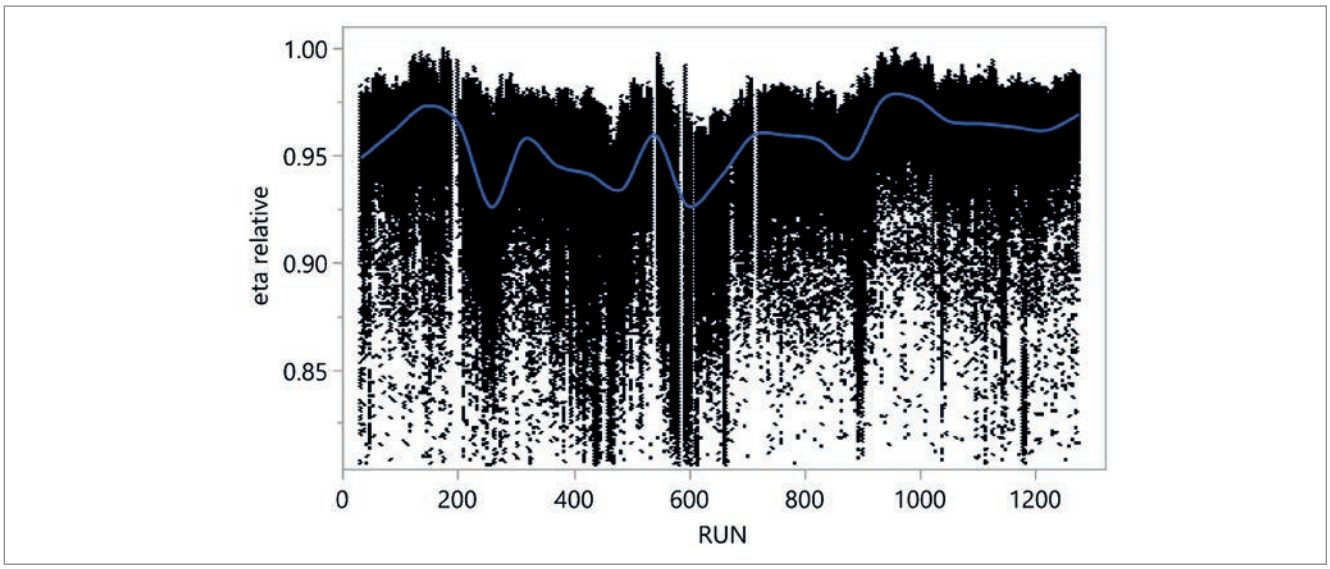
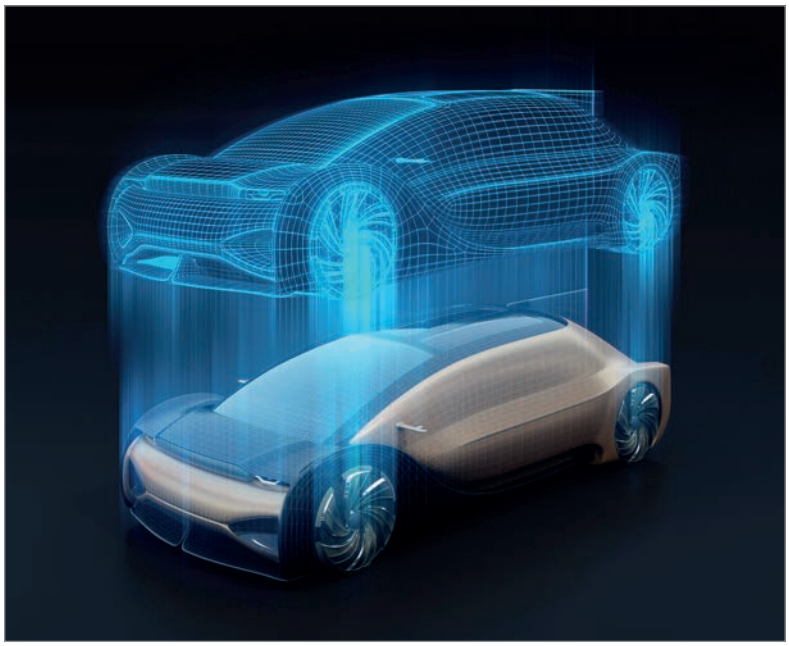


Figure 2. Sample start of a factory ramp-up, with 1 million wafers. The variations in efficiency highlight the different obstacles encountered during the ramp-up process.



Credit: Haiyin Wong/Alamy Stock Photo.

Figure 3. Digital twin representation of a car, using CAD drawings, operating details and even every screw.

self-organization: each digital twin of a plant can be addressed individually or it reports individually, with a minimal higher-level structure.

Benefits for organic line improvements

If standard interfaces or digital twins are used, data can be provided in a standard format and the devices can be linked very easily. Analyses can then be performed with software selected by the user. External experts of the user's choosing can help quickly, because they can use their own tools – uniformly for all data on the line.

The scope of the data can be expanded easily and, if desired, by the user's own digital experts. The data will form a good basis for the use of artificial intelligence (AI), be it for error analysis or for self-learning algorithms. The solutions have to be as simple as possible, even for different systems: large machines and small ones, such as sensors, must be easily hooked up.

Minimal digital twins and expansion

Digital twins can reproduce a device almost exactly: they can include computer-aided design (CAD) drawings, all components, important process parameters, manuals and much more (Fig. 3). Alternatively, only minimal information might be stored, such as the direction and current speed for a car, or etch removal and measured reflectivity for a chemical wet bench. If only alarms, etch removal and reflectivity are required, only these data need to be available. Should more data become available later, the twin must be easily expanded in due course.

"A cross-industry standard for digital twins that can be integrated with existing libraries would be desirable."

This all sounds quite complicated to implement and to coordinate among all the players in PV manufacturing. A cross-industry standard for digital twins that can be integrated with existing libraries would be desirable.

Digital twins in PV – use of a unified, cross-industry standard

The concept of digital twin in manufacturing dates back to 2003, when Michael Grieves [1] introduced it in his course on product life-cycle management. According to Grieves, a digital twin model consists of three parts: 1) the real product; 2) a virtual copy of the real product; and 3) the connections, in the form of data and information, between the real product and the virtual product.

The amount of information a digital twin might contain is wide ranging. At one end of the spectrum, there is the *rich digital twin*, which contains all available information about the product. At the other end, there is the *lightweight digital twin*, which carries only the information needed for the actual task, thus reducing the size of the model and allowing faster processing.

Digital twins are used to visualize and simulate products and systems, but they are also used to share information within the supplier's network. On the physical side, more and more data about the physical product are collected. For the greatest benefit, the real product and the virtual product should exchange information continuously throughout the product's entire life cycle. In this case, digital twins can be used to build a virtual factory replication, which constantly monitors and displays the state of the real factory.

Grieves' definition of a digital twin, consisting of a real product, a virtual representation and the connections between the two, is quite broad. The set of implementations that fall under this definition of digital twin is therefore quite diverse. And to make matters worse, there exist other concepts, such as the 'digital shadow' [2], which overlap with Grieves' definition. Kritzinger et al. [3] note that this diversity and ambiguity leads to misunderstandings, since different people have different understandings of these concepts.

Consequently, Kritzinger et al. define a classification of digital representations based on the level of integration between the physical object and the digital representation. Three classes are defined: digital model, digital shadow and digital twin. According to this classification, a *digital model* is a representation of a physical object without any automated data exchange between the digital representation and the physical object. A *digital shadow* is a digital representation of a physical object with an automated data flow from the physical object to the digital object. The digital representation is called a *digital twin*, if the automated data flow is in both directions, from the physical object to the virtual object and vice versa.

For a broad introduction of digital twins in Industry 4.0, it is necessary to have not only a consistent understanding of terminology, but also standards for the implementation of digital twins. In Germany the Plattform Industrie 4.0 [4] is developing such a standard for digital twins, called the *Asset Administration Shell (AAS)* [5]. However, in this context the term 'digital twin' is used quite broadly; specifically, a *digital twin* is defined as a 'digital representation, sufficient to meet the requirements of a set of use cases' [6]. As such, this definition covers all three classes defined by Kritzinger et al., from a pure digital model up to a fully-fledged digital twin.

The AAS concept is described in a technologically neutral form in terms of the unified modelling language (UML), in which every asset has an associated AAS. Assets can be physical assets such as machines or products, or they can be non-physical assets such as processes or computer programs.

An AAS consists of a header and a body: the header contains information to identify the AAS and the asset, whereas the body contains the data about the asset. The structure of the body is characterized by so-called *submodels*, representing different aspects of the asset. Submodels can contain properties and operations, which can be hierarchically structured. In principle, the equipment vendor or user is free to define submodels as needed, but a certain amount of standardization is beneficial. Plattform Industrie 4.0 has so far standardized the *Nameplate* submodel, which contains essential information about the asset, such as the manufacturer, serial number and year of construction [7], and the *Technical Data* submodel, which contains the sections labelled *General Information*, *Product Classification* and *Technical Properties* [8]. The implementation of a digital twin of an inline wet bench in the lab at ISC Konstanz is shown in Fig. 4.

Submodels do not have to be contained in the corresponding AAS; it is possible for them to be hosted externally, and only a reference to each submodel stored in the AAS. In addition to the submodels, the AAS concept defines a registry in which AASs and submodels can be registered. This registry allows an easy look-up of the registered AASs and submodels.

The AAS standard is accompanied by a reference implementation, which is part of the Eclipse BaSyx factory automation platform [9,10]. BaSyx is an open-source platform under the Eclipse Public License 2.0 (EPL 2.0). BaSyx provides software development kits (SDKs) for the AAS in the Java and C# languages; there is also an SDK available for C++, but this is only intended to be used for integrating existing devices.

In terms of the classification developed by Kritzinger et al., Part 1 of the AAS standard [6] defines a *digital model*. Part 2 of the AAS standard [11] defines an API for interacting with the model; this API provides the functionality for reading data from the AAS, so it can be used as a *digital shadow*. In addition, the API provides functionality for invoking operations on the AAS, thus acting as a *digital twin*. In order to fully define a digital twin, however, the interaction between the AAS and the physical asset has yet to be standardized. This gap is bridged by the Eclipse BaSyx platform, which already contains the necessary functionality. Thus, with BaSyx an AAS can be used to operate a device [10].

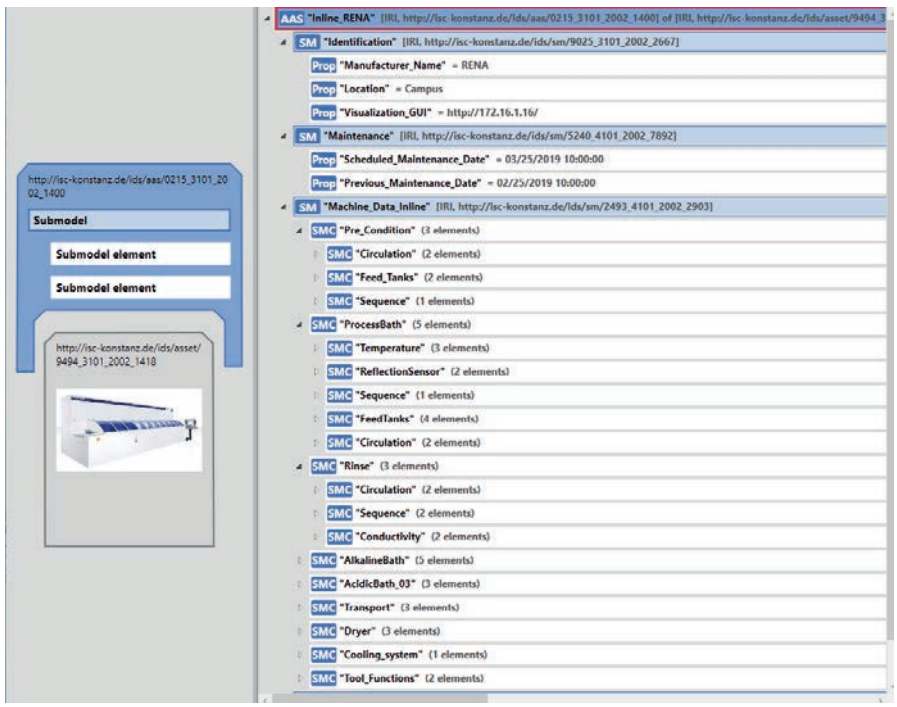


Figure 4. Implementation of a digital twin of an inline wet bench at the ISC Konstanz lab.

A twin in every machine

Every machine builder and measurement device manufacturer should offer the digital twin as standard with their products. Since the twin is based on any interface, the machine builder only has to create a twin on their PV2, OPC-UA or xml-based interface. The AAS according to 'Plattform Industrie 4.0' described above for digital twins in PV manufacturing is proposed as a standard. A minimal twin contains the nameplate, the most important alarms and the most relevant process parameters.

For demonstration purposes, all cell manufacturing facilities in the ISC Konstanz lab are currently being equipped with digital twins as part of the FlexFab 2 project. This is intended to demonstrate the control of flexible manufacturing of different cell concepts.

Additional benefits of digital twins in PV manufacturing

With digital twins, manufacturing data can be read and recipes can be changed. But there are many more applications available through the standardized structure. For instance, manuals and other documents can be regularly called up, and virtual training for operators or engineers can be carried out at the plants. Remote support is also conceivably made easier if remote maintenance software is given access to the digital twin.

Factory ramp-up can be done virtually if the digital twins have been interconnected to form a virtual factory. In addition, the factory can be operated as a 'silent factory': tasks, alarms and information are sent directly to those responsible, such as the operator's cell phone or the shift manager's smartwatch, and escalation and forwarding can be easily set up.

MES providers offer corresponding but different types of system: a 'simple' system with the connection of all equipment and access to the measurement data and data of the production plants. This can be to the extent of complete networking of manufacturing, data analysis, personnel planning, enterprise resource planning (ERP) and much more.

Ramp-up and experiments without an MES

Without an MES, ramp-up and experimentation on the line must be done entirely manually, with run sheets and transfer to Excel spreadsheets or statistical process control (SPC) tools. This may be necessary if an MES has not been purchased for a new production, if existing factories do not have an MES, or if the MES is not yet fully functional when the factory is commissioned. However, the effort required for data collection without an MES can be significantly reduced by means of a minimal integration of interfaces and databases. For ramp-up or inline experiments, samples of (for example) 100, 1,000 or 10,000 wafers are used. All data are stored, as far as possible, automatically in a central database, which can take the form of a simple SQL database.

- All plants and sensors must synchronize their clock times, which is easily accomplished automatically if they are all connected to the Internet. Otherwise, the clock times of the plants must be regularly checked.

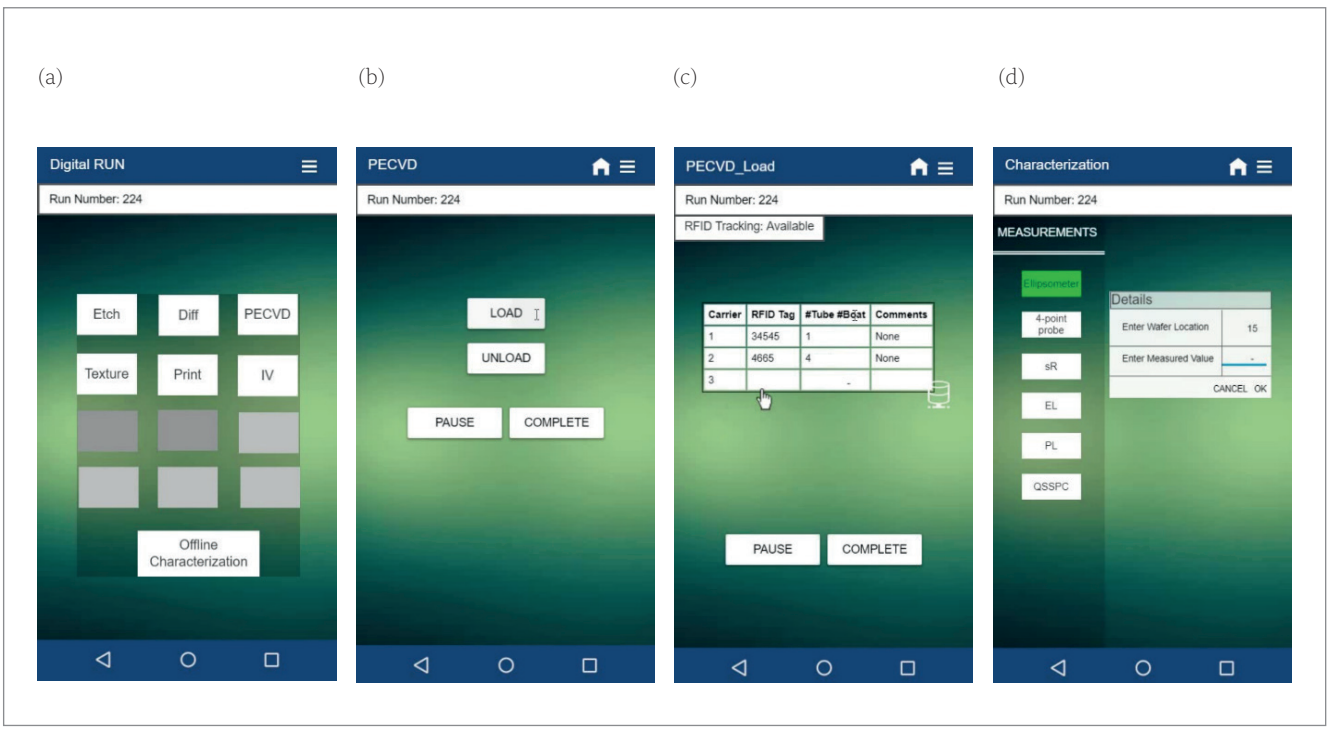


Figure 5. App developed by ISC Konstanz to follow wafers in an experiment in the absence of an MES. The tablet travels with the wafers, and operators enter values via the tablet. Screenshots: (a) choose process step; (b) load/unload form process; (c) enter details for process; (d) enter values for offline characterization.

- All equipment that generates important data (e.g. *I–V* measurement data) should be equipped with a digital interface. The data can then be easily transferred to the database using a script.

- The loading and unloading of equipment must be stored with the timestamps. For that equipment which transfers data to the database, the assignment to the experiment can be made in this way. Otherwise, data can be assigned later.

- Manually measured values are transferred to the database by hand, with assignment to the experiment and the groups.

- The transfer of measured values and the assignment of times to processes/experiments can be handled by an app that each operator runs on a tablet. ISC Konstanz has developed an app for this very purpose, which can be used during ramp-up (Fig. 5). The tablet travels with the wafers – a digital docket. However, the app must be very easy and quick to use; otherwise, operators in the factory will fail to perform the task, or they may do it carelessly and the data will be worthless. If the carriers are equipped with radio-frequency identification (RFID) tags, these can be read immediately by the tablet, thus avoiding assignment errors.

Basic MES

Basic MES options with limited functionality are available that can be used for ramp-up and experimentation; these simpler systems work much faster and are more reliable than manual solutions. The factory operator must be willing to invest in a basic MES, and the MES must be available, ready and working at the time of commissioning.

Such a basic MES must have interfaces for all systems and measuring devices and be able to store the acquired data centrally in a database that is freely accessible to the user. Some types of MES already offer virtual wafer tracking in the simplest version, which can significantly accelerate and improve ramp-up and experimentation. Self-learning algorithms and automatic experiment planning can be implemented.

It is very important that the MES works when the equipment is put into operation. To ensure this, it is best to agree when purchasing the equipment that it will be accepted and commissioned together with the interface for the MES.

The possibilities offered by a fully-fledged MES will be discussed in the section on modularization later.

Necessary standards

If all the equipment in a PV factory could be accessed in a standard fashion, the work entailed in reading data would not be very difficult. Ideally, each equipment builder supplies a digital twin of its plant in a standardized format. This standard must be recognized across industry, and so the AAS according to 'Plattform Industrie 4.0' is proposed. The digital twin can be a minimal twin, through which only important values and information about the equipment can be accessed.

When a digital twin format is not standard, the digital interface properties should at least be defined: in addition to the PV standard PV SECS/GEM, this could be according to OPC-UA or MQTT protocols.

In addition, database schemas could be prescribed for important data, which would once again significantly simplify the connections to tools for evaluation purposes.

Applications

No matter how the data are provided, the customer should be free to choose the application with which they access the data. This application must only be able to communicate with the database. The customer can then use Excel, jmp, a self-written web application or anything else, or even multiple applications in parallel, in the way that best benefits manufacturing, evaluation or ramp-up.

Growth, or what can be achieved in PV production with today's technologies

In the following two sections, the technical possibilities of digitization in PV manufacturing will be discussed. To this end, the individual possibilities of currently available MESs will be examined. In addition, the latest digitalization concepts that can be used to optimize manufacturing processes will be considered.

Fig. 6 shows the core of an MES in solar cell manufacturing, consisting of the equipment connection and manual input possibilities to allow process control and overall equipment efficiency (OEE). The advantage of this is the central material tracking of wafers. Initial extensions are quality control (QC) and SPC based on the core, which allows more detailed reports. Other components can be added later or connected as modules via interfaces.

The scalability and the flexibility to grow from a simple data-collection system (the 'basic MES' discussed above) with rough data output for central report requirements are suited to a fully data-driven business [12]. For newcomers or new factory locations in the solar industry, a balance needs to be struck between cost, effort, qualification, time and return of investment. In the case of newcomers, the complexity of the production control is often disregarded.

Preferably, the virtual factory part is built in parallel with the real factory. However, the MES is often seen by managers as less important compared

"Basic MES options with limited functionality are available that can be used for ramp-up and experimentation."

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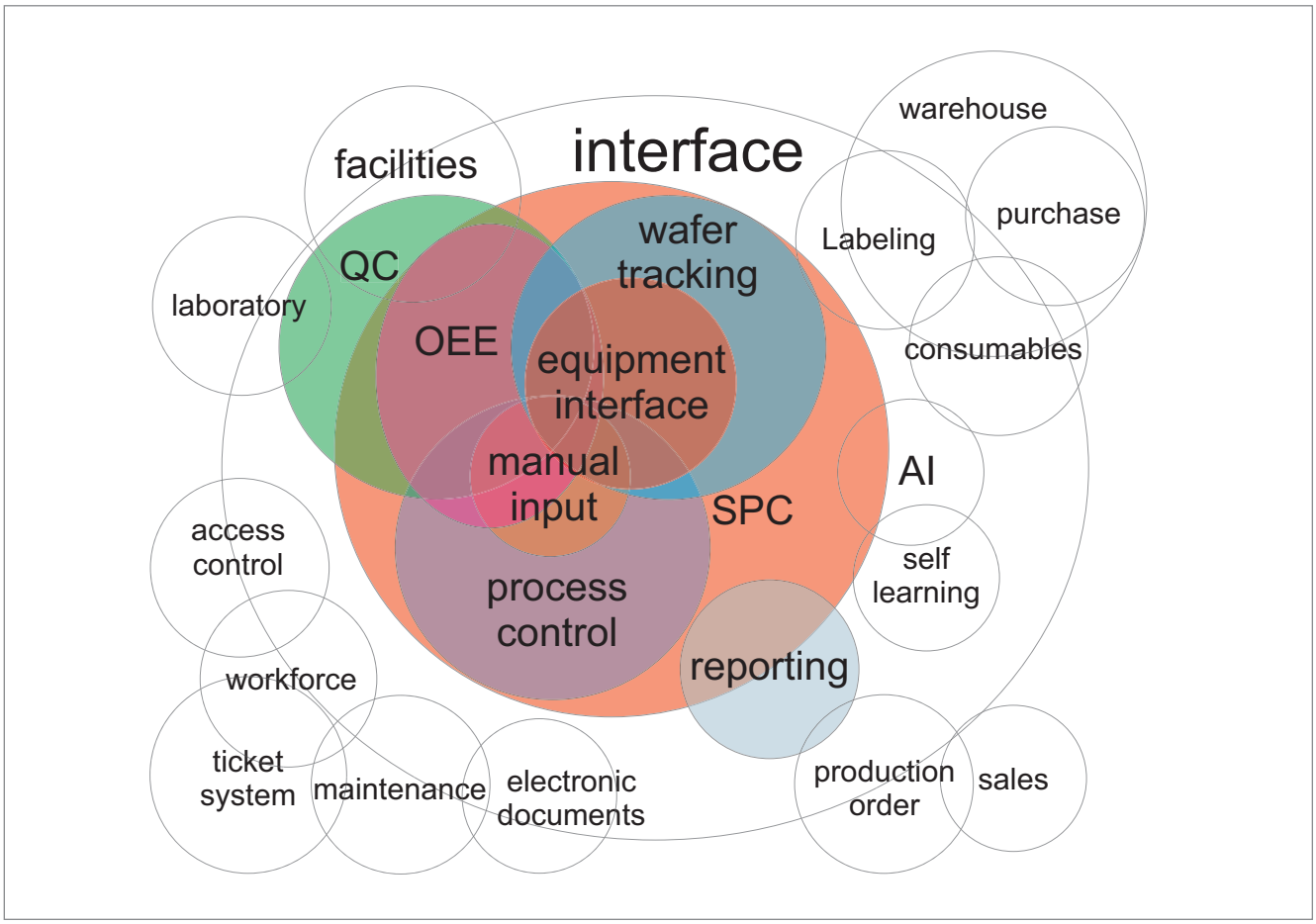

Figure 6. The core of an MES in solar cell manufacturing, with initial extensions and possible later additions or connections of other components via interfaces.

with, for example, the machines, so that not the full potential is exploited. Therefore, the core aspect of a solar cell MES, collecting SPC and OEE relevant data from each piece of production equipment, should be the initial focus. With a traditional monolithic MES, strongly coupled to the database, the selection of the database and database system is crucial, as it is unlikely that the limitations of the database structure can be overcome at a later stage. With a modern modularized approach to software development, the initial choice of database is less important, because the abstraction layers decouple the application from the underlying database.

As a full MES solution is so much more than just SPC and OEE monitoring, each vendor and industry has its own definition of beneficial add-ons and divisions between individual modules inside the MES, the ERP system above and the supervisory control and data acquisition (SCADA) systems below. In the case of full modularization and database separation (as discussed in the next section), it is possible to shift software modules between these systems or to add modules later on, depending on individual requirements. The basis for this is the possibility of running each module, or at least the core modules, separately and provide standardized interfaces between them.

The major argument against this approach is the often-feared so-called *heterogeneous IT landscape*.

"The core aspect of a solar cell MES, collecting SPC and OEE relevant data from each piece of production equipment, should be the initial focus."

In times of virtualization, interface libraries and outsourcing, this argument is overthrown by the advantages of taking, for example, specifically the best database regardless for each individual purpose.

Modularization – how far can PV production go with digitalization?

One of the basic requirements for current IT systems is their flexibility in the face of rapid development, limited resources at the beginning of a project, and unforeseen new requirements. The traditional approach for MES is a closed system from a single vendor with out-of-the-box functionality. Prima facie, the advantage of this is clear: one vendor alone is taking the risk and responsibility for the system, which is preferable, considering the numerous vendors that are already part of consortiums and projects. On the other hand, the single-vendor approach rapidly leads to a vendor lock-in. Even more likely is a system lock-in, as obviously there is no easy way of transferring the whole MES to a new system from the same vendor, if the vendor switches to using a new architecture.

On closer inspection of the data paths, it becomes clearer that these already include several different vendors and interfaces. In a classic MES, the data are most likely generated initially by analogue sensors. These signals are digitalized and transmitted via a machine internal bus to a programmable logic controller (PLC). The PLC communicates via an additional interface (either built into the PLC itself or installed as an external additional data card, box or separate HMI PC) with vendor-specific line controllers or directly with the MES. The MES then reports to the ERP system. Each of these levels of processing goes hand in hand with a data reduction and filtering stage.

The core of a classic MES is a vendor-specific relational database system (RDBMS). The flexibility and scalability are limited by the database, the onsite server capacity and the features of the MES platform. The output is then most likely limited to SPC and central recipe control, thereby leading to a reduction in onsite manpower. There is much more that can be gained from the data, depending on the specific task: external experts for data analysis could provide support if they could simply get access to the data in a freely selectable format. Recent developments in the fields of data science and analysis, such as AI, are complex and require a special approach.

A modular MES is shown in Fig. 7: while the central MES database provides compressed core information, each device registers itself in the registry. The registry stores information about data type, connection type and data storage location. Other devices can request details of data sources from the registry and directly communicate with the data source. Latency and network and server load are minimized.

Four fields in modular digital PV manufacturing can be identified. In field number one, a modular MES breaks down the single, central MES into smaller modules which have standardized interfaces in between and work more independently than software that is monolithic in nature. A monolithic MES selects and offers data to allow data handling.

Software parts are programmed in independent modules which can be run in virtual environments. Examples of modules are a piece of equipment with an interface, a digital twin, a data processing engine, an AI, an SPC system, a report system or a single industrial internet of things (IIoT) device. Each defined module, as part of the modular MES, runs in a virtual machine, independently of the hardware base. The modules are connected via standardized interfaces, with this standard being independent of vendors and preferably open source. The MES, as a central system, has to provide the hardware and storage pools, either on the premises or in the cloud. Standardized interfaces allow simple replacements of individual modules of the same type, or even parallel processing and comparison. The interface also allows the data source behind it to be easily replaced.

The second field includes modular data transformation steps, data buffer systems, predictions for data and so on; these can be intermediate modules between the original data source and the final recipient in an unlimited row. The data from sensors with more complex functions are modified, transformed, predicted or replaced by pure software code in additional modules. Instead of a direct access to the sensor data, an analysis module uses the transformed data in advance. A data source module is then a source and a recipient at the same time on the data path.

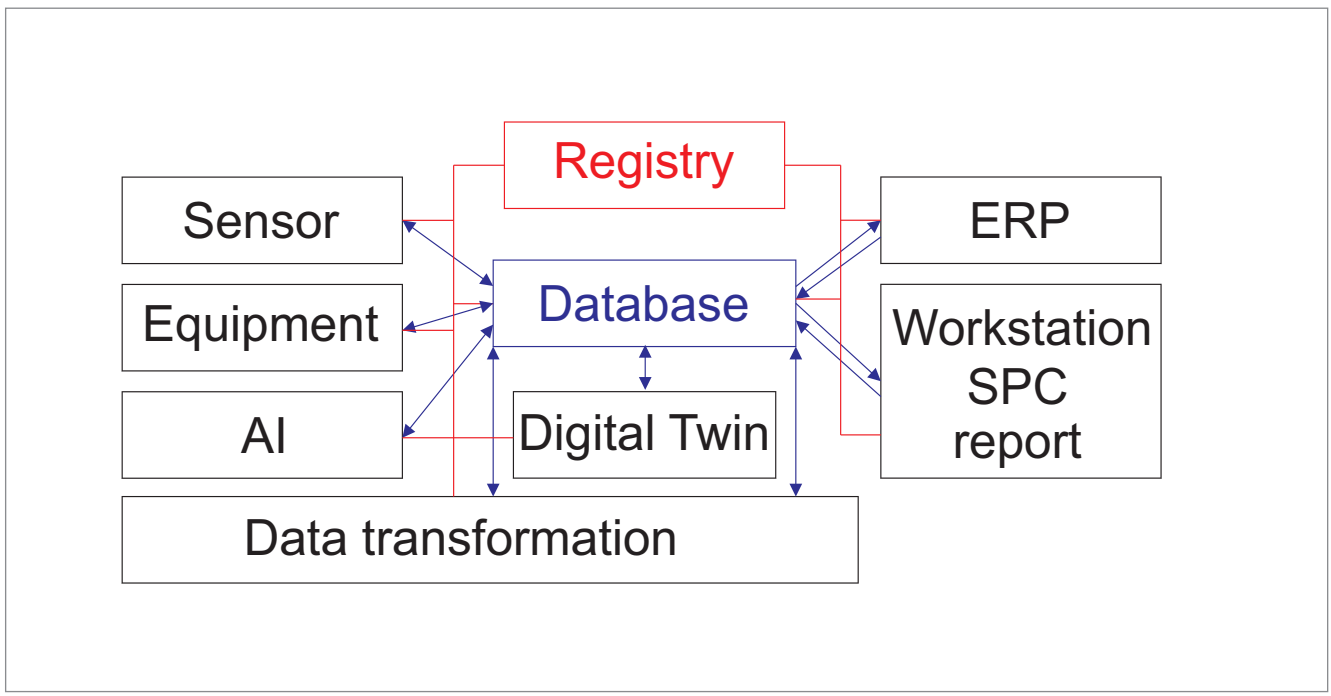

Figure 7. A modular MES.

As a consequence, it no longer matters whether physical or virtual production equipment is being run, feedback and optimizations are acquired from a human via an SPC module, or recipe adjustments are received for every batch, even during processing, via an AI [13].

In the third field, the big step forward will be the transfer from a central database to a real cloud-based system. This concept utilizes the following components. The single MES database, as the core, is divided into several databases connected together in a network of databases. Microservices, independent software instances with modules, are state of the art in many IT systems [14]. The cloud concept does not necessarily mean taking resources completely or partly from one of the three main players – AWS, Azure or Google cloud. It could also be a scalable, virtualized and flexible hardware and software resource system which is hosted locally (on the premises), but which is scalable and independent of hardware and software.

The hierarchical structure of a production sequence, from sensor to ERP system, is thereby broken down. Every module participating in the production can be both a recipient and a data source. The industrial IIoT concept describes this conversion in small steps. Each module is equal and part of a larger network. Data are equally converted, modified or generated and consumed by each player in the network. Large, spanning all sectors, active big-data specialists, such as Palantir, and/or large cloud players have defined interfaces and data structures to address the challenges of data mining.

The fourth field handles the identification of digital twins. In the future, a machine will be delivered with a digital twin as a matter of course. The digital factory will recognize it, and one will be able to easily perform a digital ramp-up that will quickly identify possible configuration errors of the complete factory.

Current standards in the solar industry – such as SECS/GEM, EDA or OPC-UA – still mainly target the SPC as the final data output, which is fine for manual data mining. A big-data approach, however, needs to go one step further. In addition to the current interfaces, a direct pathway between data source and recipient has to be defined.

The complete transformation of an MES into a modular system allows additional freedom in design and data flow. A modular virtualized system not only includes existing standards, but also guides real-time data from sensors and other players into a data pool. This system makes use of cloud-compatible interfaces, thereby generating an up-to-the-minute system. It benefits from modular Industry 4.0 steps with digital twins, AI and further current developments [15]. This system could directly register communication channels and request metadata such as communication protocols from the central MES core. Each participant is therefore recorded in the registry, either manually or automatically in advance. Subsequently, the digital twin of, for example, a diffusion furnace is automatically recognized as such and integrated into the infrastructure with all connections, just as if it were physically placed in the line. By means of a direct pathway between any sensor in the furnace and the AI, even pure, unstructured sensor data will be available and can be fetched as needed by the AI. Therefore, a direct connection to the machine internal network will be established without limitations by digital interfaces.

Only through an overall transition of an MES as proposed in these four fields can the development from a pure measurement collection system to a platform take place, and the rapidly increasing data pool be transformed to allow data mining and to generate an efficient and rapid 'digital payback'.

Wafer tracking: real and virtual

The most interesting part in an MES for solar cell factories is the material flow and its tracking. Besides all secondary material flows from chemicals, water, pastes, etc. there is one linear main material flow. The wafer is a clearly defined unit going through all the steps and conversions in solar cell production, starting from polysilicon up to panel installation on a roof. The wafer is therefore the primary material to follow and track in cell production. Batch tracking, where a batch may consist of 1,000 to 40,000 wafers, is the minimum requirement for all productions worldwide.

Some advanced factories adopt the approach of single-wafer tracking, in which each individual wafer is tracked at each production step. All measurement data are coupled either directly or via timestamps to the wafer ID. Two different ways of tracking are possible. In the first method, each wafer is marked by laser individually on the front or back side (as described by Q CELLS [16]), while the second option involves marking the edges of the wafer in the silicon brick. In each production step, both possible types of wafer mark can be read out by cameras. The tracking accuracy is claimed to be above 95% over the full production process, and even in the final module the wafer marks can be read out several years after production. Although this system allows total traceability based on hardware marks over a long period of time, it requires specialized hardware, and is only feasible if the data is required to be available for many years or if the data is to be used to significantly improve cell and PV module quality.

Another approach is to only track wafers virtually, in which case the wafer marks are not mandatory, but still helpful for checks and adjustments. Virtual wafer tracking requires the tracking of all transportation steps inside and outside of all

"The most interesting part in an MES for solar cell factories is the material flow and its tracking.

production equipment, handling and measurement systems, and of external and internal transportation. In this way, small batches of about 100 wafers are tracked by IDs in the form of barcodes, QR codes or RFID chips in carriers or boxes.

A physical wafer that is acknowledged by a piece of equipment for the first time receives an ID from that equipment; this will most likely occur during the incoming inspection. The ID, together with position and timestamp information, is reported to the virtual wafer tracking instance (usually the MES). Simultaneously, the equipment transfers the wafer ID to the connected automation. The automation then binds the wafer ID to the position inside the batch, herein defined as the carrier and the carrier ID. The position of the wafer is now defined. Measurement data, recipes or other sensor data are transferred separately and coupled virtually to the wafer ID.

In the next step, the equipment which processes complete carriers without any wafer handling just manages the carrier ID and informs the MES about all the process steps. Equipment that either processes individual wafers or requires specific boats for wafers has its own particular automation. The automation involves opening the batch both physically and virtually, and requesting the wafer ID and position of each ID in the carrier after reading the RFID code on the carrier. A virtual copy of the automation then handles each wafer ID in registers. These registers represent belts, robots, buffers or even boats inside the process equipment. The wafer ID is thereby treated like the real wafer; this requires full access to all automation information, which is best provided by the automation manufacturer itself. After all the steps, the wafer is returned to a carrier with an ID. The automation thus binds wafer position and ID to a carrier ID once again and closes the batch.

In inline processes, such as wet-chemical inline equipment, the wafer ID is handed over with a timestamp and position, in this case in the lane at the entrance, to the process equipment. The process equipment then takes over the responsibility for the wafer ID itself, as it automatically transfers the wafers at a well-known speed to the exit. The equipment subsequently transfers the information back to the automation. In this method, the MES does not follow the wafer itself, but only gets informed of the wafer ID's process timestamp.

The MES is independent of the equipment binding the process information to the wafer ID. Only measurement values from single wafers are directly bound to the wafer ID. Wafers that are absent because of breakage, delays or mismatch are treated as lost, and this information is stored for a certain period of time. A wafer that is rediscovered somewhere along the line without a wafer ID is assigned a wafer ID by the equipment itself; each piece of equipment is therefore allocated a unique range of IDs for this purpose.

The disadvantage of virtual wafer tracking is the dependency on each single automation and process in order to carry out the internal wafer tracking properly, as there is no control stage. At the same time, the identification of a single cell inside a PV module on a roof is also only virtually possible, requiring virtual wafer tracking, even between the different production steps of the cell and module and within the module production. To the authors' knowledge, this has not been achieved until now. The accuracy of the virtual wafer tracking approach can also be more than 90%, depending on the accuracy of each piece of equipment and production flow.

Outlook into the factory of the future

Individual paths of each wafer

Industry 4.0 is used for manufacturing individual products in other industries (Lot Size One). At first, this would seem an outlandish approach for solar cells and modules. Individual prediction and individual pathfinding, however, can also be useful in PV manufacturing, such as in the preparation of wafers from ingot areas with lower lifetimes in processes with optimized conditions (e.g. in a diffusion with better gettering properties). Q CELLS, in particular, has demonstrated the advantages of wafer tracking: typically, the position of the wafer in an ingot has a bearing on the final efficiency of the solar cell [16].

Currently, all process steps in solar cell production aim for a homogeneous result. Dosing in wet-chemical equipment is adjusted to target homogeneous etching, texturing or cleaning results over the bath lifetime and from bath to bath. Tubes in thermal equipment are designed in such a way as to guarantee that the result over the full boat is as homogeneous as possible. Target values with tolerances for wafer interior, wafer to wafer and batch to batch definitions aim for an acceptable amount of deviation over the full production.

In the sorter at the beginning of the line, during the incoming inspection, wafers can be separated into different classes. These classes are preferably already treated slightly differently in the later processes, otherwise the expectations of cell efficiency in the corresponding campaigns are lower. At the end of the line, the sorter separates the cells according to their efficiency or colour into bin classes. The obvious goal is to obtain homogeneous results with even treatments using a single recipe set; in reality, however, the results are more heterogeneous. Depending on the process, between 5 and 10% of wafers are produced with different base resistivities, treated differently in wet-chemical baths and within the average values for wafers from different positions within the boat (wafer to wafer over the boat).

Current MESs track and can even select the correct recipes for batches. The next step is to optimize each recipe and, depending on the results

after each process cycle, make adjustments to the recipe. The optimization of each recipe and each tube by SPC, as well as by AI, on the basis of the optimum conditions for each batch is already close to being realized.

The following step is to not only track each wafer, but also actively guide the wafer through the production. Instead of binning groups, each wafer is treated individually. On a complete decision matrix there would be an optimum process flow for each wafer, which is of course adjusted after each process step. The MES creates groups of wafers which are processed together in batch processes, but the position of each wafer in the batch is not random. On the basis of the trend in baths and boats, each wafer is individually assigned its position in each process step. Buffers and bins in the automation are used to manipulate the wafers actively into the perfect position. Some examples are given next.

On the assumption that the first and last wafers in a diffusion boat are more likely to yield a lower cell efficiency and will be sorted out in the sorter after printing, it might be advantageous to already put in this position a wafer that is almost out of spec because of its base resistivity. Therefore, a low-quality wafer will also be allocated a low-quality position in the diffusion. As the risk of low printing quality is higher when a screen change in the printer is imminent, this particular wafer could also be printed during this period. In this way, low-quality wafers are given low-quality positions, and the risk of good wafers going to waste is reduced. In contrast, the best-performing cells are created by always putting the best cell in the best position. An alternative goal could be to keep the efficiency distribution as narrow as possible, thus, conversely, to process bad wafers in further-optimized processes.

The additional benefit of this system of actively positioning the wafers will be that the recipes for each group of wafers can be optimized on the basis of their needs. Process windows, which currently have to match a higher bandwidth of incoming wafer conditions, can be significantly tightened in the case of granular bin sorting before each process step. This benefit can already be realized, with positive SPC results. It is achieved via clear rules, replacing the assignment of bin classes to single recipes by mathematical factors for time, temperatures and other process parameters. The flexible boundaries create an unlimited number of flexibly defined bins and batches with different recipes. Instead of bins with predefined boundaries, bins of a defined size with minimized scattering are created for each process step. When a large number wafers are being considered, the total scattering will become small.

The next logical step would be to use this flexibility in AI concepts. A virtual wafer is passed in advance through a virtual cell factory. Each wafer is then guided in its preferred batch with optimized recipes at each step for deciding the best place for it.

"A self-learning PV factory can independently improve its production."

Self-learning factory: physical models vs. AI concepts

A self-learning PV factory can independently improve its production. On the one hand, it can improve the quality of individual cells or modules, while, on the other, it can improve throughput and yield. Physical models or AI can be used for this purpose – or a mixture of the two.

For instance, a physical model can match the thickness of the silicon nitride layer to the reflective properties of the wafers, which have different properties as a result of the different saw damage after etching. In contrast, AI can be used to investigate which influencing parameters have an impact on the cell results. The common outcome of these two scenarios is that the manufacturing process can be dynamically adjusted.

An example of self-learning manufacturing is the use of automated experiments in production lines: in other words, a system that can independently suggest and perform a statistically significant design of experiment (DOE). This will allow, for example, new metallization pastes or new metallization screens to be investigated quickly and in an optimized manner. For this purpose, boundary conditions are defined for the system, such as the limits of the snap-off or the permitted firing parameters. Thus, the line independently plans the experiment, carries it out and outputs the optimum possibilities of a new paste or an alternative screen for the current cell concept. It conducts the experiment in the shortest possible time and with the minimum loss of yield in the current production.

Self-learning FlexFab

RCT and ISC are working together on a factory concept in which different cell and module concepts can be manufactured in parallel. The proportion of the respective solar cells fabricated is required be variable, so that more solar modules of one type or of the other can be produced, depending on the request. For example, a FlexFab can produce passivated emitter and rear cells (PERCs) for the mass market and n-type back-contact ZEBRA cells for the rooftop market.

The wafers follow individual paths in a FlexFab, and production is monitored and controlled by digital twins. This type of manufacturing is currently being implemented at ISC Konstanz on a pilot-line scale. Self-learning aspects are considered in a FlexFab, so that the performance of the modules and factory throughput are constantly improving.

It is important to always be mindful of the manufacturing costs. The paths of the wafers are optimized and the manufacturing processes are

combined to such an extent that the additional cost for the FlexFab production of PERC cells is only 0.6%, compared with a purely PERC production.

Acknowledgement

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Industrial n-type PERT cells with doped polysilicon passivating contacts: Past, present and future

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Abstract

The industrial n-type passivated emitter and rear totally diffused (PERT) cell with doped polysilicon passivating contacts is an attractive next-generation technology, as average efficiencies above 24% have recently been demonstrated in mass production. Despite these very promising efficiencies, several factors are limiting this technology's rapid adoption in mass production, including the relatively higher cost of manufacturing equipment and the increased process complexity, leading to lower manufacturing yields. This paper provides a short overview of historical developments, presents the main approaches in mass production today, discusses potential process simplifications, and briefly touches upon a key topic for the future, namely reducing the silver (Ag) consumption per cell.

Introduction

Since 2014, the crystalline silicon (c-Si) PV industry has experienced a learning rate (LR) of over 25%, meaning that the manufacturing cost (in $/W) of PV modules has decreased by over 25% for every doubling of the cumulative production. As explained in detail in Chen et al. [1], this accelerating LR is due to several factors, including the massive scaling-up of manufacturing, mainly in China, rapid improvements in cell and module efficiencies, and a strong alignment between the players around a domestic supply chain for high-throughput tools and key materials (polysilicon, wafers, Ag pastes, glass, etc.).

Although China has been a major contributor to the rapid development of PV manufacturing, it does not mean that PV manufacturing outside China cannot be competitive. This is because high labour costs are becoming less significant with increased automation and throughput, while shipping costs are becoming proportionally more important with falling manufacturing costs and the increasing relevance of factors such as CO_2-footprint [2]. Furthermore, PV manufacturing is becoming a strategic industry for ensuring a domestic supply of low-cost and sustainable energy, and for creating thousands of jobs across the value chain.

The upshot of all this is a renaissance of PV manufacturing in all major PV markets (Europe, USA, India, etc.). For 2021, BloombergNEF analysts are forecasting global PV installations to increase from 132GW in 2020 to somewhere in the range of 160 to 209GW, and standard PV modules prices to fall by a further $0.02/W, to $0.18/W [3]. Consequently, higher solar cell efficiency has never been so important as it is today, since it impacts the manufacturing cost (in $/W) of every other component. Similarly, higher module efficiency is key to reducing the overall PV system costs and ultimately to achieving a lower levelized cost of electricity (LCOE) [4].

"Next-generation cell technologies capable of efficiencies well above 24% will be required in order to push average module efficiencies above 22%."

Most c-Si PV modules being sold today are based on gallium-doped (p-type) industrial passivated emitter and rear cells (PERCs) with local aluminium doping [5]. The average efficiency of industrial PERC in mass production has been improving steadily by ~0.5%$_{abs}$ per year, from ~20% in 2013 to ~23% today (see Fig. 1), thanks to hundreds of small improvements in materials, equipment and processing. PERC efficiencies of ~23.5% appear feasible in the coming years, as already demonstrated by Hanwha Q-cells at the pilot-line level [6]. However, progress beyond 23.5% is expected to be slower and more laborious, as explained in several roadmaps [5,7–9].

In parallel to improving PERC efficiency, the PV industry has recently embarked on making several rapid changes in cell and module design in order to increase module power, reduce cell-to-module losses, decrease manufacturing costs and improve energy yield. These changes include:

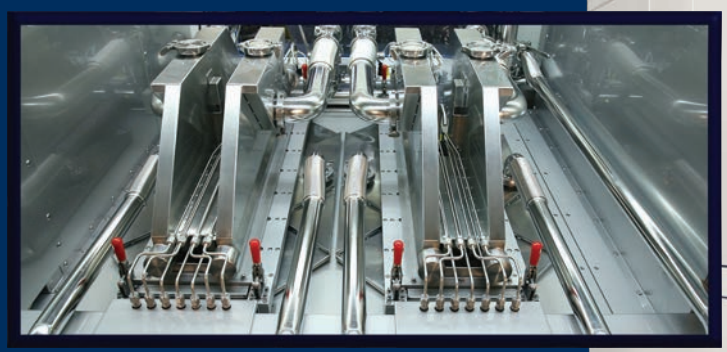
- Rapid push towards larger wafer formats (up to 210mm).
- Reduction of interconnection losses by cutting cells in half or smaller pieces and introducing multi-busbar concepts.
- Reduction (or even elimination) of cell gaps to improve packing density.
- Introduction of bifacial cell and module designs to collect light from both sides.

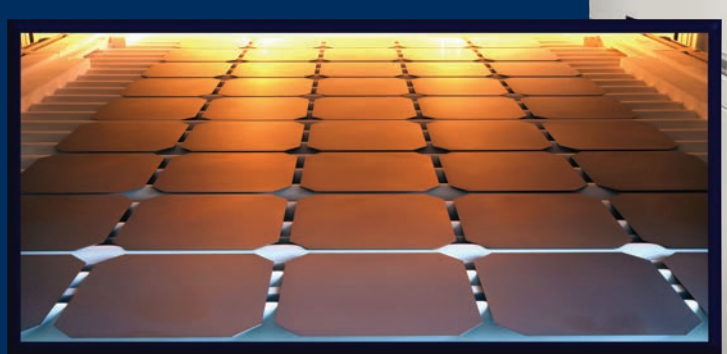
As a result of all these changes, the typical efficiency of monofacial PERC modules has quickly improved from 18–19% in 2018 to 20.5–21.5% today, while the

PASSION ■ INNOVATION ■ TECHNOLOGY

APCVD

ONE system - MANY advantages





- Single side coating
- Small footprint:
  Length 165 inches | Width 82.5 inches
- 5000+ WPH Throughput
- Extremely low cost of ownership
- In-situ doping: boron or phosphorous
- Can accommodate any size wafers without modification
- Attractive in-line configuration with wet tunnel oxide process and in-line anneal
- High deposition temperature means less anneal time is required
- Simple to achieve very high levels of in-situ doping
- Excellent uniformity
- Films can be deposited in any sequence

best bifacial PERC modules now have efficiencies in the range 20.4–21.3%.

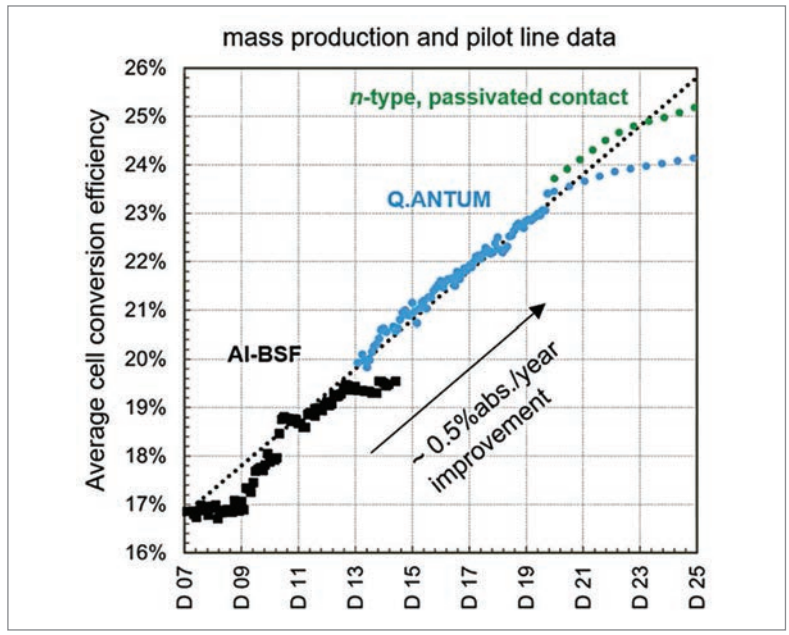
With the progress in PERC cell efficiency expected to be more tedious and major improvements in module design being implemented, next-generation cell technologies capable of efficiencies well above 24% will be required in order to push average module efficiencies above 22%. Several technologies – including passivated emitter and rear totally diffused (PERT), silicon heterojunction (SHJ), interdigitated back contact (IBC) and, more recently, perovskite/silicon (Pk/Si) tandem – have been on the radar of the International Technology Roadmap for Photovoltaic (ITRPV) and of the R&D community for several years [10,11].

Among those technologies, n-type SHJ and n-type PERT with doped polysilicon (poly-Si) passivating contacts seem to be gaining the most traction among PV manufacturers, as average efficiencies above 24% have recently been demonstrated in mass production, while record efficiencies around 25% have been achieved in pilot lines [12–15]. Both of these technologies rely on the concept of carrier-selective contacts to improve cell efficiencies [16] and reduce temperature coefficients [17]. Moreover, both technologies typically feature narrow Ag grids on both sides, resulting in higher bifaciality values than with PERC.

Finally, the use of high-quality phosphorus-doped (n-type) substrates helps to drastically reduce the magnitude of light-induced degradation (LID) and light- and elevated temperature-induced degradation (LeTID) [18]. The combination of lower temperature coefficients, higher bifaciality and lower LID/LeTID enables substantial improvements in the energy yield of a PV system.

Compared with n-type SHJ technology, a major benefit of n-type PERT cells with poly-Si passivating contacts is their compatibility with conventional high-temperature processing, including diffusion, plasma-enhanced chemical vapour deposition (PECVD) of hydrogenated silicon nitride layers (SiN_x:H), firing-through of Ag pastes, and standard soldering of flat ribbons or wires. This allows one to benefit from gettering and hydrogenation to significantly improve bulk lifetimes [19,20]; it also enables manufacturers to tap into a well-established supply chain for equipment/materials and a talent pool that is familiar with high-temperature processing.

On the other hand, there are several factors that limit the rapid adoption of n-type PERT cells with poly-Si passivating contacts. These constraints include the relatively higher cost of manufacturing equipment, the increased process complexity, leading to lower manufacturing yield, and the higher Ag consumption per cell than that for p-type PERC. Note that the relatively higher cost of n-type substrates can also be an additional factor, but this can be mitigated by moving to thinner substrates than for p-type cells [21].



Source: Faes et al. [66]

Figure 1. Average cell conversion efficiencies achieved at Hanwha Q-cells since December 2007 with Al-BSF and subsequently with Q.ANTUM (PERC) technology. The values beyond 2021 represent projections based on internal roadmaps.

Several PV manufacturers are now adding significant production capacity for n-type PERT cells with poly-Si passivating contacts, as significant progress has been made in the last few years on all fronts (materials, equipment, process simplifications). This paper briefly reviews historical developments, examines the main approaches in mass production today and presents potential process simplifications. A key challenge for the future – the reduction of Ag consumption per cell – is also discussed.

Historical developments

The idea of implementing doped poly-Si passivating contacts to improve carrier selectivity in silicon devices is not new. A short overview is given in Fig. 2 and in the paragraphs below. A more detailed overview can be found in a recent review by Hermle et al. [22].

Originally used as an emitter in heterojunction transistors [23], the doped semi-insulating polysilicon (SIPOS) approach enabled impressively high open-circuit voltages (V_{oc}) of 720mV to be achieved on p-type in 1985 [24]. However, approaches based on doped poly-Si have fallen out of favour with most research groups because of the high process complexity and the narrow process window. In 2005, Swanson stated that new contacts with a "J_o of less than 5fA/cm² that make good majority carrier contact" were needed, one for electrons and one for holes [23]. Not long after, SunPower successfully implemented passivating contacts in its Maxeon GEN3 IBC cells, with the V_{oc} improving from 680–690mV (GEN_2) to 710–730mV (GEN3) [25]. Continuous improvements allowed SunPower

"There are several factors that limit the rapid adoption of n-type PERT cells with poly-Si passivating contacts."

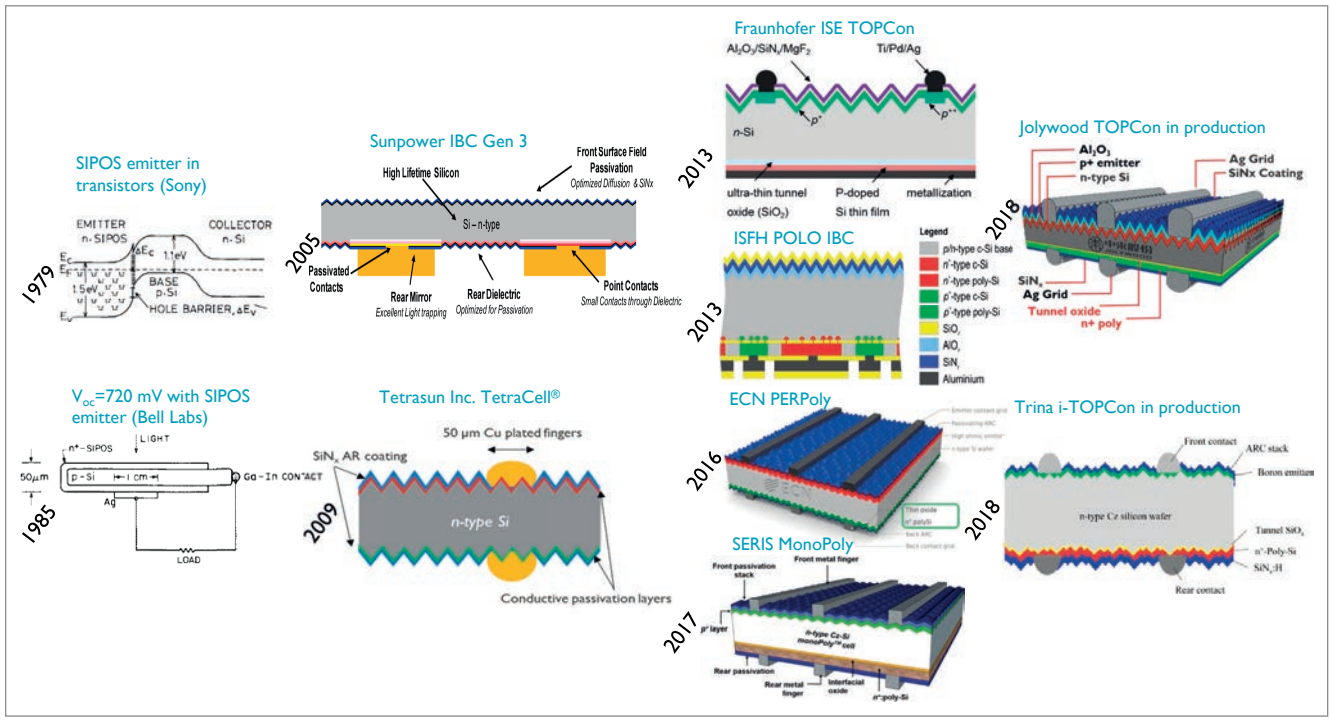


Figure 2. Short overview of the historical developments of poly-Si passivating contacts, leading to high-volume production of n-type cells with tunnel oxide passivated contact (TOPCon) technology.

to demonstrate, in 2016, IBC cells with a total area efficiency above 25% (V_{oc} = 737mV, J_{sc} = 41.33mA/cm², *FF* = 82.7%) [26].

In 2009, TetraSun began the development of its TetraCell, featuring conductive passivation layers and Cu-plated contacts on both sides [27]. After its acquisition by First Solar, TetraSun's technology was transferred into production. Median efficiencies of 21.9% (V_{oc} = 701mV, J_{sc} = 39.3mA/cm², *FF* = 79.5%), and a best cell efficiency of 22.8% (V_{oc} = 718mV), were demonstrated in 2016 [28]. In the same year, however, the TetraSun line ceased production, as First Solar decided to concentrate on its core thin-film business.

The interest in doped poly-Si passivating contacts exploded when Fraunhofer ISE and ISFH started to report very swift progress in their tunnel oxide passivated contact (TOPCon) and polysilicon on oxide (POLO) IBC concepts, using laboratory processes (photolithography patterning, 2×2cm² designated cell area, etc.) and materials (float-zone (FZ) silicon, evaporated contacts, etc.). Fraunhofer ISE introduced its TOPCon technology in 2013 [29]. Initially, a best cell efficiency of 23.7% (V_{oc} = 703mV, J_{sc} = 41.0mA/cm², *FF* = 82.2%) was obtained using a homogeneous p^+ emitter at the front and a rear passivating contact stack consisting of a 1–2nm chemical oxide, 20nm-thick n^+-doped poly-Si, and evaporated Ag. Continuous developments and the implementation of a selective p^+ emitter structure at the front led to 25.1% efficiencies in 2015 [30]. Further optimization culminated in Fraunhofer ISE reporting, in 2020, efficiencies of up to 25.8% on n-type FZ, and of even up to 26% on p-type FZ, which is the current world record for two-side-contacted cells, thanks to lower surface recombination and lateral transport losses [31].

ISFH started to develop processes to form n^+- and p^+-doped POLO also around 2013 [32]. Several years of development led to ISFH announcing in 2018 a POLO IBC on p-type FZ with an efficiency of 26.1%, which remains the world record for a p-type Si solar cell to date [33]. The process to form POLO contacts in these cells consisted of:

1. A dry oxidation to grow a 2.2nm-thick oxide.
2. Low-pressure chemical vapour deposition (LPCVD) of amorphous Si (a-Si).
3. Phosphorus and boron implantations (to form n^+ and p^+ regions respectively).
4. Annealing above 1,000°C to break up the oxide layer and form contacts between the poly-Si and c-Si via pinholes.
5. Evaporating aluminium (Al).

To bridge the gap between laboratory and high-volume manufacturing, many R&D institutes and companies started to develop methods to implement poly-Si passivating contacts using low-cost materials, equipment and processing steps. In 2016, ECN was among the first to report large-area (6") bifacial n-type PERT cells [34]. ECN's PERPoly cells featured 200nm-thick n^+ poly-Si passivating contacts on the back side, formed by means of industrial LPCVD and $POCl_3$ diffusion equipment from TEMPRESS, and screen-printed fire-through Ag contacts on both sides. This was quickly followed by SERIS, who explored both industrial LPCVD and PECVD approaches to form the n^+ poly-Si in MonoPoly® bifacial n-type PERT cells.

Contact formation using fire-through Ag pastes was initially challenging, as the pastes partly consumed the n^+ poly-Si layers, leading to relatively high recombination current densities in

the metallized areas ($J_{0,met}$) of 386fA/cm² and non-optimum specific contact resistivities (ρ_c) of around 3–5mΩ·cm² [35]. The rapid development of dedicated Ag pastes allowed this issue to be addressed, with excellent $J_{0,met}$ ~ 35fA/cm² and ρ_c ~ 1–2mΩ·cm² values reported only two years later by different authors [36]. By 2018, Meyer Burger in collaboration with SERIS reported 6" bifacial n-type PERT cell efficiencies of up to 22.6% with V_{oc}~700mV using a single piece of inline PECVD pilot-line equipment to form the tunnel oxide and deposit n^+-doped Si prior to recrystallization in a tube furnace [37].

Around the same time, several companies (Jolywood, Trina Solar, LG and REC among others) started mass production of (6") bifacial n-type PERT with poly-Si passivating contacts by retrofitting old lines and adding only a few new tools to save on capital expenditure (CAPEX) and compete with low-cost bifacial PERC products. Two early examples are shown in Fig. 2, with Jolywood choosing to upgrade several standard n-PERT lines using a LPCVD + phosphorus implantation + tube annealing approach to form the n^+ poly-Si [38], and with Trina Solar choosing to upgrade a p-type multi Al-BSF line using a LPCVD + $POCl_3$ diffusion approach to form the n^+ poly-Si [39].

Approaches in mass production today

Today several companies are mass producing n-type PERT cells and modules with passivating contacts [36,37,40,41]. In addition, a number of Tier 1 producers have earmarked existing p-PERC production lines for a future upgrade to TOPCon to limit CAPEX [39]. Like the beginnings of p-type PERC mass production around 2014, the biggest challenge for the industrialization of n-PERT with poly-Si passivating contacts is to find the right process sequence and associated set of tools/materials leading to high efficiency, high yield and low manufacturing cost.

In Fig. 3, the main processing steps for n-PERT cells with poly-Si passivating contacts using different approaches based on LPCVD, PECVD, APCVD or PVD of a-Si are schematically compared, alongside a reference process sequence for bifacial p-PERC. For total cost of ownership (TCO) and LCOE comparisons, the reader is referred to the excellent work recently published by Kafle et al. [42], who compared slightly different approaches to the ones listed in Fig. 3.

The reference bifacial p-PERC process starts with texturing, typically in a batch tool, prior to emitter formation in a $POCl_3$-based low-pressure tube furnace. This is usually followed by a laser processing step to form a selective emitter (SE) and reduce contact recombination losses [8]. This step is listed as optional, as some companies have developed a leaner and more cost-effective process without SE (for one example, see Altermatt et al. [5]). Next, rear emitter removal and chemical edge isolation are achieved by means of single-side etching (SSE) in an inline tool, which also removes the phosphosilicate glass (PSG) and cleans wafers prior to subsequent processing. This can be followed by an optional dry oxidation in a tube furnace to improve passivation and contacting [43]. Typical alternatives include chemical oxidation (either in the SSE tool or separately) or plasma oxidation which can be combined with the subsequent deposition of all passivation layers in a so-called *3-in-1* inline PECVD tool [44]. The exact deposition sequence for the AlO_x/SiN_x passivation layers at the rear and the single-layer (or multi-layer) SiN_x at the front depends on the equipment chosen (PECVD, PEALD, ALD, APCVD). Finally, local laser contact openings (LCO) are formed prior to the metallization sequence, which typically consists of multiple screen-printing steps (rear Ag pads, rear Al grid, front Ag grid), fast-firing in a belt furnace, and a hydrogenation step to reduce the impact of LID and LeTID.

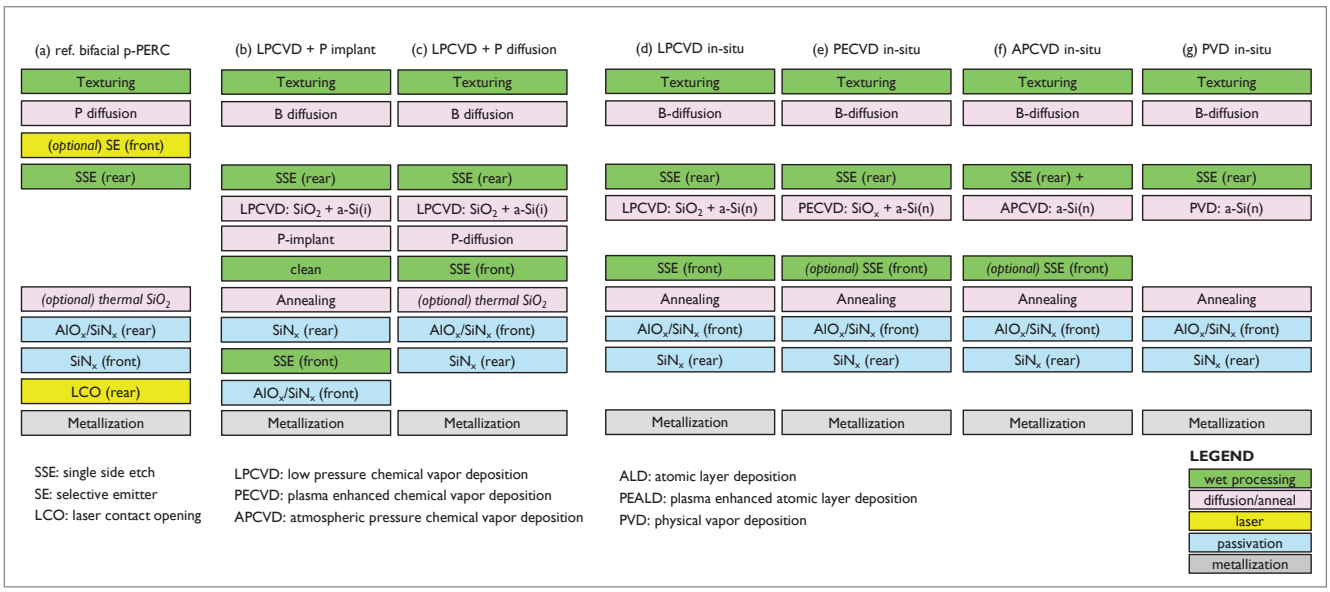


Figure 3. Main cell processing steps for (a) reference bifacial p-type PERC, (b–c) mainstream n-PERT with poly-Si passivating contacts (TOPCon) in mass production, and (d–g) other approaches used in mass production or being evaluated in R&D. The same legend colour code as in Kafle et al. [42] has been chosen, to help with direct comparisons.

"LPCVD is the most mature approach today for the mass production of n-PERT with poly-Si passivating contacts."

The approaches initially used by Jolywood and Trina Solar to mass produce their TOPCon cells are shown in Fig. 3(a) and Fig. 3(b), respectively. Both start with texturing, p^+ diffusion (typically in a BBr_3-based low-pressure tube furnace), and rear SSE in inline tools similar to those for p-PERC. The borosilicate glass (BSG) formed during p^+ diffusion is typically kept intact during the rear SSE step to protect the p^+ emitter during the subsequent front SSE of poly-Si. An LPCVD tube furnace is used to form a thin (1–2nm) tunnel oxide by in situ dry oxidation at low temperatures and to deposit a thick (100–200nm) layer of a-Si. The LPCVD a-Si layer properties are influenced by deposition pressure, silane (SiH_4) concentration and, most significantly, deposition temperature [45].

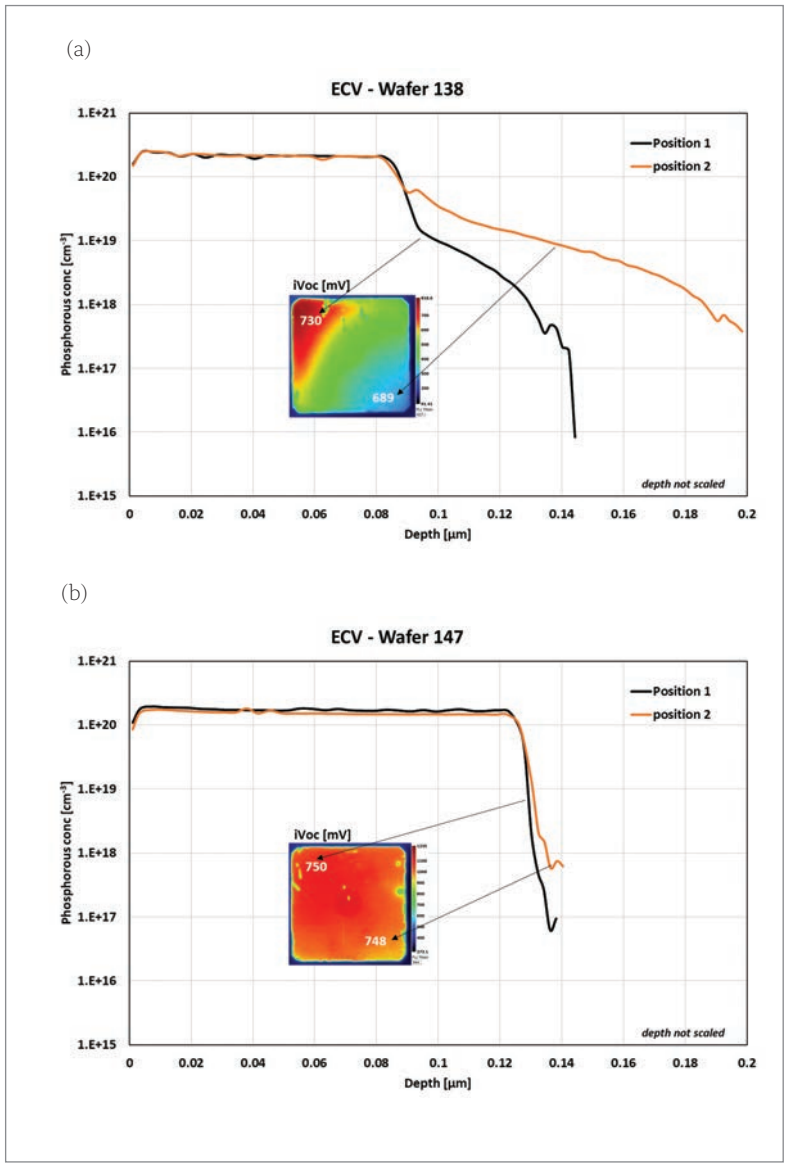


Figure 4. Electrochemical capacitance–voltage (ECV) of n^+ poly-Si layers formed at imec using LPCVD for in situ dry oxidation + a-Si deposition and $POCl_3$ ex situ doping: (a) non-optimized dry oxidation recipe, leading to n^+ tail diffusion and non-uniform iV_{oc} (as shown in the photoluminescence (PL) image insert); (b) optimized dry oxidation recipe, resulting in uniform ECV profiles and iV_{oc} along the wafer.

LPCVD a-Si deposition is followed by n^+ ion implantation (P implantation) at Jolywood (since it retrofitted existing n-PERT lines using P implantation) and $POCl_3$-based diffusion at Trina Solar (since it retrofitted exiting Al-BSF lines using this tool). The P implantation step presents the advantage of being truly single sided, which helps to obtain good reverse-current (I_{Rev}) characteristics and allows, after rear SiN_x deposition, the use of standard inline or batch cleaning tools for the front SSE of poly-Si (undoped). On the other hand, P implantation suffers from limited throughput and requires additional cleaning and annealing steps to form the n^+ poly-Si. The $POCl_3$-based diffusion allows the formation of the n^+ poly-Si in a single high-throughput step, but requires a dedicated tool for the front SSE step, typically using a sequence of alkaline etching (to remove n^+ poly at the front and the edges) and cleaning steps that is critical to achieving high performance and good I_{Rev} characteristics.

Surface passivation typically consists of Al_2O_3/SiN_x at the front and SiN_x at the rear, with the exact layer composition and deposition sequence depending on the set of equipment chosen (as with p-PERC). Finally, the metallization sequence (and equipment required) is typically the same as that for p-PERC, with the exception that Ag grids are printed on both sides. As with p-PERC and n-SHJ cells, several R&D institutes and companies have reported significant efficiency gains when using an extra hydrogenation step after the fast-firing process on TOPCon cells [46,47]. Consequently, the extra hydrogenation step is increasingly becoming standard in all high-efficiency Si cell concepts prior to testing/sorting.

As just explained, LPCVD is the most mature approach today for the mass production of n-PERT with poly-Si passivating contacts. Major advantages of LPCVD include:

- The availability of industrially-proven high-throughput tools from multiple vendors.
- Good thickness control along the wafer and the boat.
- Pinhole-free layers.
- The option of easily creating constant doping profiles using in situ doping (see next section).

On the other hand, LPCVD poses several challenges, such as:

- Lower deposition rates (r_{dep}) than with PECVD or PVD.
- The need for a front SSE step, as the deposition is inherently performed on all wafer sides.
- Deposition on the sidewalls, leading to the risk of tube cracking (hence requiring frequent tube replacements).
- Difficulties in creating a very uniform tunnel oxide along the wafer, which is critical to achieving uniform lifetimes and control carrier selectivity.

An example of LPCVD is shown in Fig. 4, where non-optimized in situ dry oxidation led to phosphorus tail diffusion, causing increased Auger recombination losses and hence lower iV_{oc}. This was correlated to thinner oxide formation at the bottom of the M2-format wafer (sitting in a diamond-shaped boat) than at the top. Such non-uniformity issues are highly dependent on the recipe used and the LPCVD tool design (boat, etc.), and are expected to become worse for larger format wafers (M10, G12 formats).

Potential process simplifications

An initial potential process simplification that is being considered is the addition of n^+ doping gas (PH_3 diluted in N_2) during LPCVD. A major benefit of performing LPCVD doping in situ is that the subsequent P diffusion is no longer required. While a post-annealing is still considered to be necessary for achieving high carrier selectivity [48], it allows the elimination of the optional oxidation step prior to passivation (cf. Fig. 3(d) and 3(c)) by adjusting the post-annealing ambient conditions. Moreover, the n^+ poly-Si properties (active doping, thickness, etc.) can simply be tuned by adjusting the LPCVD in situ and post-annealing recipes. An example of this is shown in Fig. 5, where the active doping ($N_{D,act}$) of LPCVD in situ doped n^+ poly-Si layers is simply controlled by changing the PH_3 flow [49]. A major challenge with LPCVD in situ doping is obtaining a sufficiently high r_{dep} and $N_{D,act}$ at the same time. Nevertheless, by adjusting the deposition parameters it is possible to simultaneously achieve an r_{dep} of 4.7nm/min and an $N_{D,act}$ of 1.3E20cm^{-3} [48], which are of the same order as the results reported by Stodolny et al. for LPCVD ex situ [45].

A second potential process simplification that is being considered by a number of institutes and companies is the use of a process sequence based on PECVD in situ (see Fig. 3(e)). It has already been explained briefly that Meyer Burger together with SERIS reported in 2018 a 22.6% n-PERT cell efficiency using a single piece of inline PECVD equipment to form the tunnel oxide (by plasma oxidation) and deposit n^+-doped Si prior to recrystallization in a tube furnace [37]. Major benefits of this approach include:

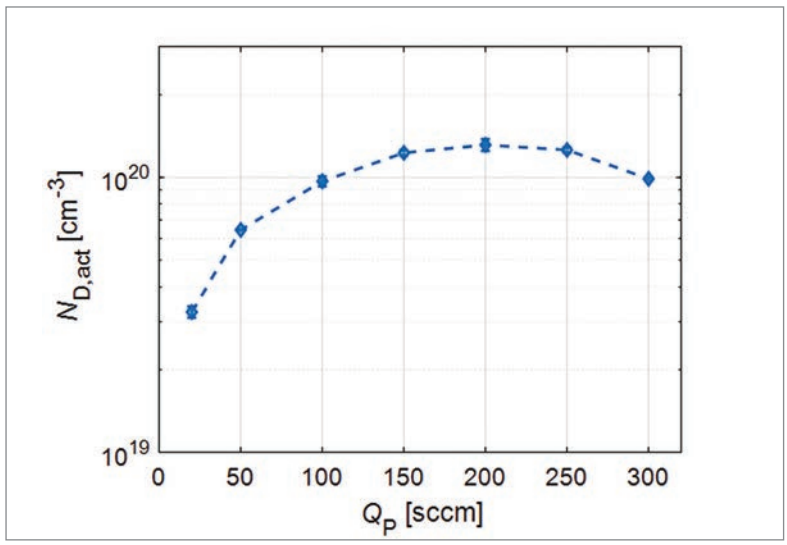
- Tunnel oxide thickness uniformity is easier to control than in a tube furnace.
- High deposition rates >1.5nm/s can be achieved.
- Layer properties can easily be tuned by adjusting deposition parameters (e.g. temperature, gas flows, pressure, plasma power).

One of the major challenges with inline PECVD at low temperatures is to avoid blistering in thick layers (typically >100nm is required to obtain low $J_{0,met}$ with firing-through Ag metallization) because of the inherently high hydrogen concentration in the deposited a-Si layer. Solutions to this include using additional gases during the deposition process (such as CH_4, NH_3 or N_2O) to incorporate small amounts of carbon (C), nitrogen (N) or oxygen (O) and improve the blistering behaviour [50,51]; however, this also impacts the electrical properties of the layers (bandgap, active doping, mobility, etc.), which can make optimization difficult. Another option is simply to design the inline PECVD equipment to allow depositions at temperatures above 500°C, as already done by Meyer Burger [37] and shown recently by others [52]. In a similar approach, it is also possible to modify tube PECVD equipment to deposit thick and uniform a-Si(n) at high temperatures, with cell results >23% recently demonstrated by Feldmann et al. [53].

One major advantage of tube PECVD is that it is used extensively in the crystalline PV industry for the deposition of passivation layers (AlO_x, SiN_x, etc.) at high throughputs and low cost. Compared with inline PECVD, it might be more challenging to implement uniform plasma oxidation to form the tunnel oxide with tube PECVD, and hence companies might instead choose to perform chemical oxidation during the rear (SSE) step before PECVD. Avoiding wrap-around of a-Si(n) layers is considered a major technological milestone for both inline PECVD and tube PECVD manufacturers, as this would allow the front SSE step to be skipped.

A third process simplification option is to use inline atmospheric pressure chemical vapour deposition (APCVD) to deposit doped a-Si layers at high throughputs. The main benefit of APCVD compared with LPCVD or PECVD is that the deposition is done at atmospheric pressure and hence it works without gate chambers (only gas curtains), vacuum chambers (no pumps) or plasma sources. The basic idea for the

"There is an enormous potential for process simplifications (and associated CAPEX reductions) in the mass production of n-PERT cells with poly-Si passivated contacts."



Source: Firat et al. [49].

Figure 5. Active doping (from Hall measurements) of LPCVD in situ doped n^+ poly-Si as a function of PH_3 flow (Q_P).

Superior quality control for PERC, TOPcon, and HJT cell manufacturing

- QC for multi- and c-Si based solar cell manufacturing
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deposition of a-Si layers is the thermal dissociation of SiH_4 in an atmosphere with very low oxygen concentration (hence the use of N_2 gas curtains), and the precipitation of the silicon atoms as a-Si on the heated wafer. By adding doping precursors (PH_3, B_2H_6, etc.) in the SiH_4 flow it is possible to deposit doped a-Si(n) and a-Si(p) layers, as reported by Merkle et al. [54]. As with inline PECVD, the move to larger format wafers (M10, G12) could possibly be easier with APCVD than with LPCVD. One major challenge is designing the injector heads to achieve uniform and high-throughput deposition without clogging (particularly as the presence of even small amounts of oxygen can lead to silica powder formation). As in the case of PECVD, avoiding any wrap-around deposition is considered a major milestone that is needed in order to skip the front SSE step. Presumably, APCVD is already in use by companies such as SunPower or LG to mass produce IBC cells with passivating contacts. It remains to be seen if APCVD will gain significant market share in the mass production of n-PERT cells with poly-Si passivating contacts.

A fourth simplification option is to use inline physical vapour deposition (PVD) to deposit doped a-Si layers at very high throughputs. Inline direct current (DC) PVD is already used extensively for the deposition of transparent conductive oxides in SHJ cells, with the latest equipment capable of throughputs greater than 10,000 wafers per hour with M6 wafers, or greater than 6,000 with G12 wafers [55]. Apart from the very high throughput capability, major advantages of PVD include:

- Excellent thickness uniformity.
- Solutions already exist for achieving single-side deposition without any wrap-around.
- No hazardous gases (SiH_4, H_2, PH_3, B_2H_6, etc.) are required, unlike with other techniques.

PVD, however, is still a relatively novel technology for forming poly-Si passivated contacts. Excellent results have been demonstrated using laboratory techniques, such as radio frequency (RF) co-sputtering of undoped silicon and boron targets [56] or electron beam (EB) co-evaporation from silicon and gallium phosphide effusion sources [57]. As regards the more industrial approach of performing high-speed DC sputtering from a single P-doped silicon target, results obtained so far have been limited to iV_{oc} < 700mV as a result of insufficient dopant activation, the difficulties in procuring Si targets with a dopant density well above 1E20cm^{-3}, and possibly some sputtering damage [58].

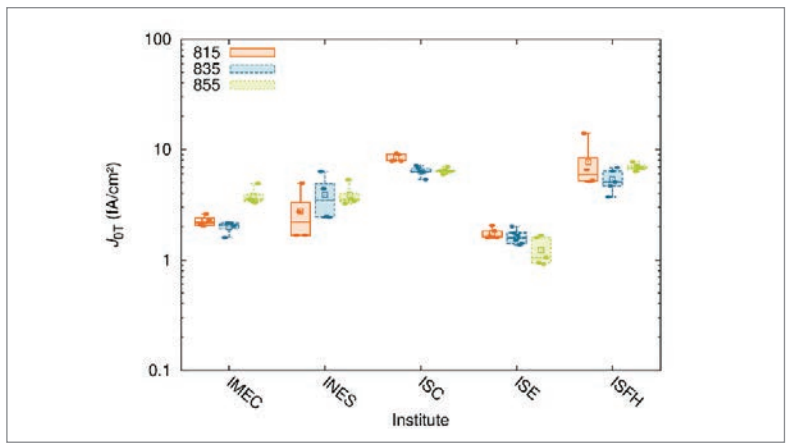
Overall, there is an enormous potential for process simplifications (and associated CAPEX reductions) in the mass production of n-PERT cells with poly-Si passivated contacts. Excellent progress has already been made using the various approaches listed above, and other promising depositions techniques, such as plasma oxidation and plasma-assisted in situ doping deposition (POPAID) or plasma-enhanced atomic layer deposition (PEALD), are also being investigated to form n^+ poly-Si layers. For example, Jolywood recently reported excellent cell results >24% with yields >97% using its new POPAID technology in pilot lines [59]. This technology has the potential to drastically reduce the CAPEX required for new lines, bringing it on par with (or below) that needed for bifacial p-PERC while enabling significantly higher cell efficiencies. In a joint experiment involving different approaches (LPCVD ex situ, LPCVD in situ, PECVD in situ) to form n^+-doped TOPCon layers (tunnel oxide, n^+ poly-Si, dielectric capping) in industrial tools, all the partners were able demonstrate excellent $J_{o,total}$ (see Fig. 6), $J_{o,met}$ and ρ_c values using screen-printed Ag contacts [60]. This clearly shows that the equipment and know-how to produce >24% n-PERT cells with poly-Si passivated contacts are quickly maturing. This is expected to lead to a rapid reduction in CAPEX and manufacturing costs in the coming years because of increased competition across the supply chain, similar to what happened with p-PERC between 2014 and 2018 [1].

Approaches to reducing Ag consumption

One of the major challenges for cost-effective manufacturing of PV modules is to reduce Ag consumption, as it now represents 10% of the overall module cost structure [61]. This is expected to get worse as annual PV production ramps up towards the terawatt level by the end of the decade [62]. According to the latest version of the ITRPV 2020 [10], the median consumption value in 2020 was 90mg of Ag per cell (G1 format), representing 17mg/W (assuming a median 21% efficiency based on Al-BSF and PERC market shares in 2020). As a result, the 132GW of PV modules produced in 2020 consumed at least 2,244 tonnes of Ag or about 9% of the global Ag production.

The PV annual consumption of Ag is expected to increase because: 1) the quantity of PV modules produced per year is increasing faster than manufacturers can reduce Ag consumption per cell; and 2) higher efficiency concepts, such as TOPCon

"Ag consumption now represents 10% of the overall module cost structure."



Source: Fellmeth et al. [60].

Figure 6. Total dark recombination current density $J_{o,total}$ for an n-type bulk and two unmetallized TOPCon layers.

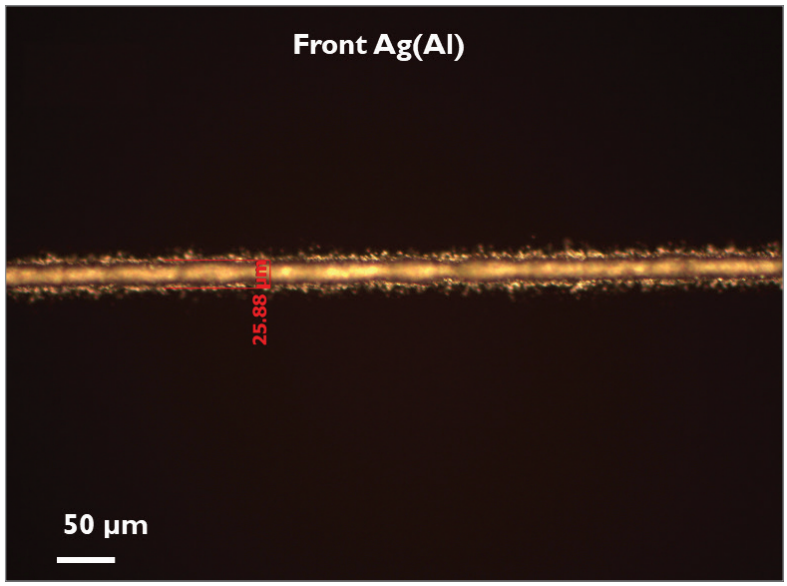
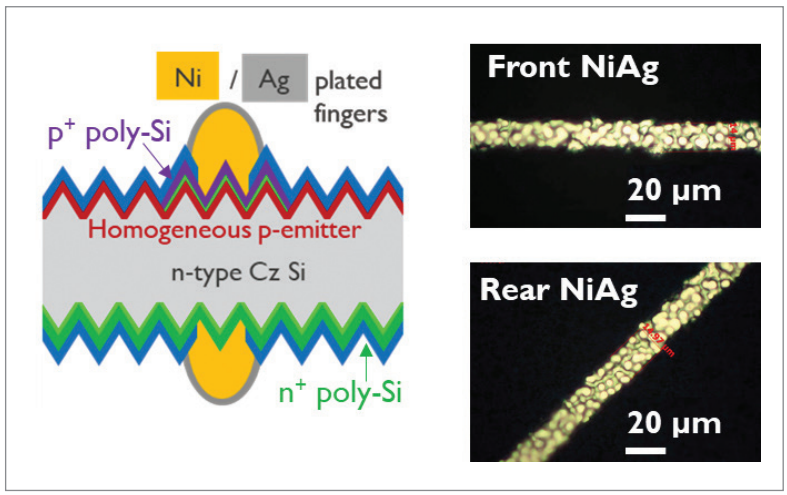


Figure 7. Example of fine-line screen printing at imec using commercially available screen-printing equipment and Ag(Al) paste to contact the p^+ emitter.



Source: Singh et al. [68].

Figure 8. Schematic of an n-PERT cell with blanket n^+ poly-Si at the rear, selective p^+ poly-Si at the front and plated NiAg fingers on both sides.

and SHJ, which consume more Ag per cell since Ag is printed on both sides, are gaining market share. That is why it is critical to rapidly reduce the Ag consumption per cell in those concepts compared with the 2020 median values of 150mg/cell (TOPCon) and 200mg/cell (SHJ) given in the ITRPV [10].

A first approach to reducing Ag consumption per cell is to print narrower fingers and implement multi-busbar interconnection technologies. Excellent progress with industrially available screen-printing equipment, standard mesh screens and commercially available Ag pastes has been achieved at imec in recent years [63]. This is now leading to ~25µm fingers, as shown in Fig. 7, and Ag consumption of around 50mg per side (M2 format) for TOPCon cells made at imec. Similar progress has also been reported by other companies [5,8] and R&D institutes such as Fraunhofer ISE using conventional screen printing [64] or parallel dispensing technology [65]. However, despite the excellent progress made in the last few years it will be difficult to reduce Ag consumption per cell to below 30mg per side (M2 format) without adopting busbarless interconnection technology, such as Smart Wire Contacting Technology (SWCT) currently employed with SHJ cells [66].

A second approach to significantly reducing Ag consumption per cell is to implement plated contacts. At imec, an innovative and simple, contactless, co-plating method has been developed with very low Ag usage per cell, since it relies on plating nickel (Ni) and a thin Ag capping layer [67]. This approach was recently adapted for n-PERT cells with poly-Si contacts implemented on both sides (see Fig. 8), to further reduce contact recombination losses; initial results obtained on test wafers were promising [68]. Not long ago, excellent progress was also reported using sequential nickel/copper/silver (Ni/Cu/Ag) plating in bifacial n-PERT cells with n^+ poly-Si at the rear side; efficiencies of up to 22%, limited by front-side recombination losses, were achieved [69]. With further developments, both the Ni/Ag and Ni/Cu/Ag plating approaches should be capable of reaching efficiencies above 24% and Ag consumption less than 10mg/cell; this would lead to Ag levels below 1.7g/W, representing a tenfold reduction with respect to the reported industry median in 2020.

> "n-PERT cells with poly-Si passivating contacts are an attractive technology for pushing average module efficiencies above 22% in the coming years."

Conclusions

Given that the progress in p-PERC cell efficiency is expected to be more tedious and that major improvements in module design are already being implemented, n-PERT cells with poly-Si passivating contacts are an attractive technology for pushing average module efficiencies above 22% in the coming years. This paper has provided a short overview of historical developments that led to average efficiencies of above 24% being recently demonstrated in mass production. The main approaches in mass production today were presented, together with potential process simplifications. Finally, a key challenge for the future was discussed, namely the reduction of Ag consumption per cell.

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About EnergyVille

EnergyVille is a collaboration between the Belgian research partners KU Leuven, VITO, imec and Hasselt University in the fields of sustainable energy and intelligent energy systems. EnergyVille develops technology and knowledge to support public and private stakeholders in the transition to an energy-efficient, decarbonized and sustainable urban environment.

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Mechanical strength of HJT cells: Raising the bar in achieving a low wafer thickness in production

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Abstract

The mechanical strength of silicon cells remains one of the main issues in the PV industry, as it requires a balance of conflicting interests between the upstream and the downstream segments. With margins squeezed along the supply chain, cell prices are becoming increasingly under pressure, but the ongoing reduction of wafer thickness raises concerns over the growing risks of production losses and reliability issues. Owing to low-temperature processing, a fully symmetric structure and fewer production steps, silicon heterojunction technology (HJT) is able to tolerate thinner wafers as compared to mainstream passivated emitter and rear cell (PERC) technology. Indeed, the latest achievements in a successful shift from 180µm- to 150µm-thick wafers in mass production of HJT cells gives manufacturers more confidence and brings certain economic benefits. At the same time, however, the rapid scaling-up of the wafer size to M6, M10 and G12 will face immense challenges with regard to a reduction in wafer thickness. The race for higher cell efficiency and greater power output from PV modules of standard dimensions will demand new R&D approaches and equipment suppliers. In this paper, an even greater reduction in wafer thickness, down to 130µm, is evaluated, and the critical steps in terms of breakage rates in cell and module production processes are reviewed. Finally, the mechanical stability and reliability of these thin HJT cells in glass–backsheet and glass–glass module types are addressed.

Introduction

Today silicon heterojunction technology (HJT) holds efficiency records for double-side-contacted [1] and rear-side-contacted [2] Si solar cells fabricated from industrial-size Cz wafers. According to the recent International Technology Roadmap for Photovoltaic (ITRPV) report [3], in mass production, HJT technology yields the highest efficiencies for solar cells with a conventional metallization grid and will continue to hold onto the leading position in efficiency among Si PV technologies until at least 2030 or, in other words, until the development of cost-effective tandem-Si-based technology.

Unfortunately, despite the outstanding efficiency, the market share of HJT solar cells is limited because of higher production costs than for passivated emitter and rear cell (PERC) technology, which recently became mainstream. The higher cost of HJT modules can be offset by the advantages of HJT cells, such as lower temperature coefficient < 0.3%/°C, higher open-circuit voltage ≥ 740mV and greater bifaciality ≥ 90%, providing additional gain in solar module performance via higher output at operating temperature, lower resistivity losses and better harvesting of scattered light arriving at the rear side of bifacial modules. These advantages, however, are usually not so evident for investors. Thus, achieving a decrease in production costs is necessary in order for HJT to increase its market share.

"Achieving a decrease in production costs is necessary in order for HJT to increase its market share."

Like other high-efficiency Si PV technologies, HJT requires n-type monocrystalline silicon (mono Si) wafers, which are now up to 10% more expensive than p-type wafers used in mainstream Si PV technologies [4]. Despite the contribution of Si wafers to the total module costs having a decreasing trend in the last few years, it still constitutes about one-third in the case of monocrystalline wafers. A reduction of the Si wafer thickness is therefore one of the most obvious ways to decrease the costs of HJT modules. Moreover, as the production of mono Si from feedstock to ingots demands more than fifty per cent of the total energy required for solar module production [5], using thinner wafers for HJT cells makes this technology more competitive in the countries which have committed to "making finance flows consistent with a pathway towards low greenhouse gas emissions", within the framework of the UNFCCC Paris Agreement.

The effect of wafer thickness on the HJT cell parameters has recently been studied at the laboratory level and in pilot-line production by various research groups [6–8]. It has been found that, thanks to outstanding amorphous silicon passivation quality providing surface recombination rates as low as 1cm·s^{-1} [8], the increase in open-circuit voltage and the reduction in bulk recombination rate can compensate the effect of a reduction in short-circuit current when using thinner wafers [6]. As a result, there are almost no differences in the efficiencies of HJT

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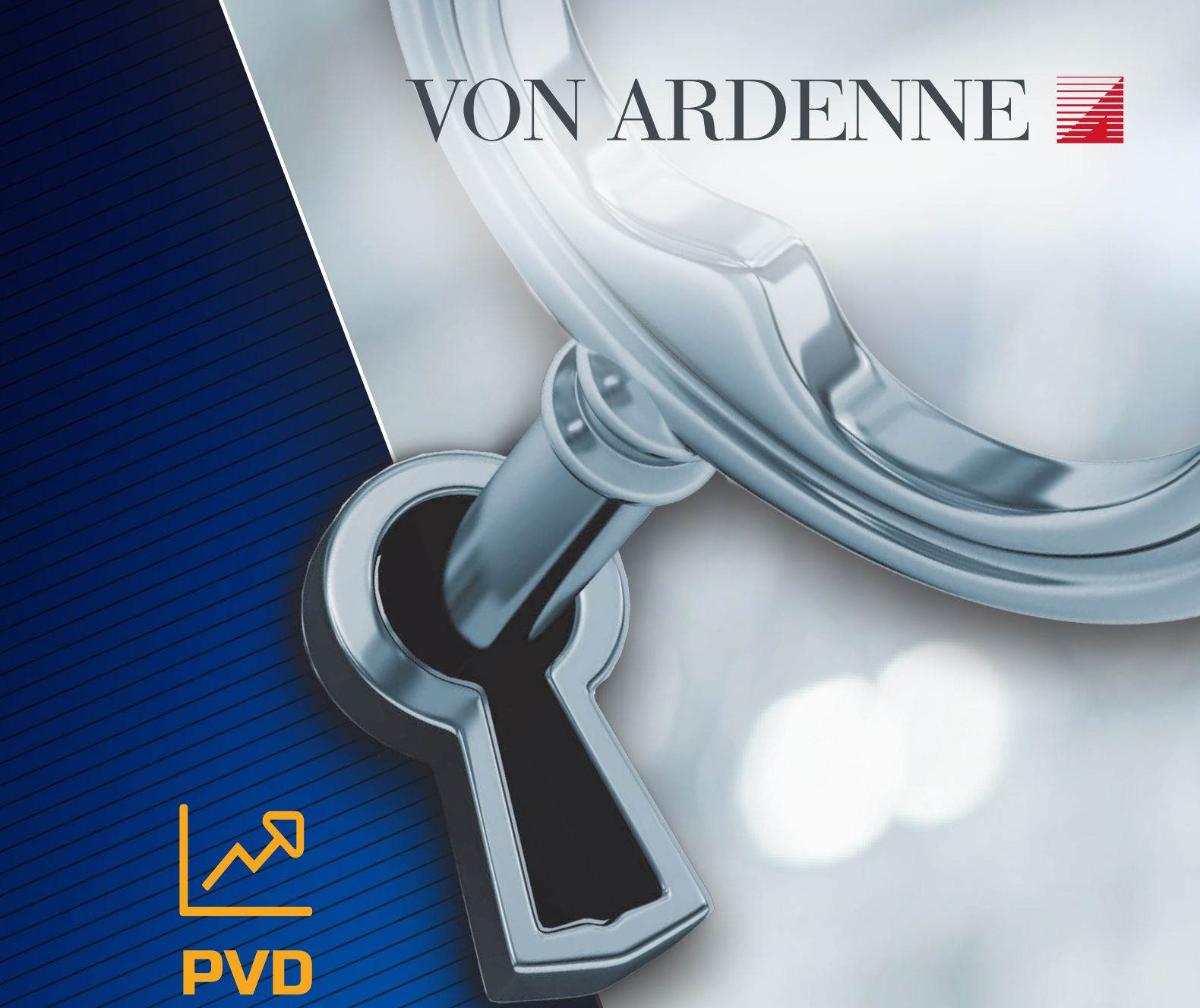

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cells manufactured from wafers with thicknesses ranging from 160µm down to 90µm, while maximal efficiencies for cells with optimized light trapping were observed with around 100µm-thick wafers [7]. Such findings are consistent with the data obtained for the cells manufactured on Hevel's production line.

As Hevel completely switched to 150µm-thick c-Si wafers in production as early as 2018 [9], the focus of the study reported in this paper will be on further reductions of wafer thickness. A comparison of the electrical parameters for bifacial cells of different thicknesses is shown in Fig. 1(a). As expected, the transition to a 130µm wafer thickness leads to a reduction in I_{sc} by 0.1A, with a simultaneous increase in V_{oc} by about 2–3mV, as compared to the 150µm wafer thickness, and results in an overall cell efficiency loss of about 0.2%$_{abs}$.

In contrast to the cell data, thinner wafers lead to a power gain at the module level. Fig. 1(b) shows the parameters of the glass–backsheet modules assembled from the HJT cells of different thicknesses. As one can see, the additional absorption of light reflected from the white backsheet compensates the current losses, so that the cell-to-module (CTM) losses become smaller for thinner wafers, with an overall gain of up to 3W for a 60-cell module.

As there is no significant reduction in efficiency at the cell level, the main issues for the implementation of thin Si wafers in mass production are related to the yield losses caused by higher wafer breakage rates, and the lower mechanical strength of the cells affecting a module's long-term durability. This paper presents a brief overview of the experience in using wafers of thicknesses of 150µm and below for HJT cells and the production of modules at Hevel [9,10], followed by a discussion of the general status of related issues.

Mechanical cell strength and production yield losses

Wafer handling at all production steps and the thermal stress induced by cell processing are considered the main reasons for cell breakage during manufacturing. Since HJT cell manufacturing requires fewer production steps

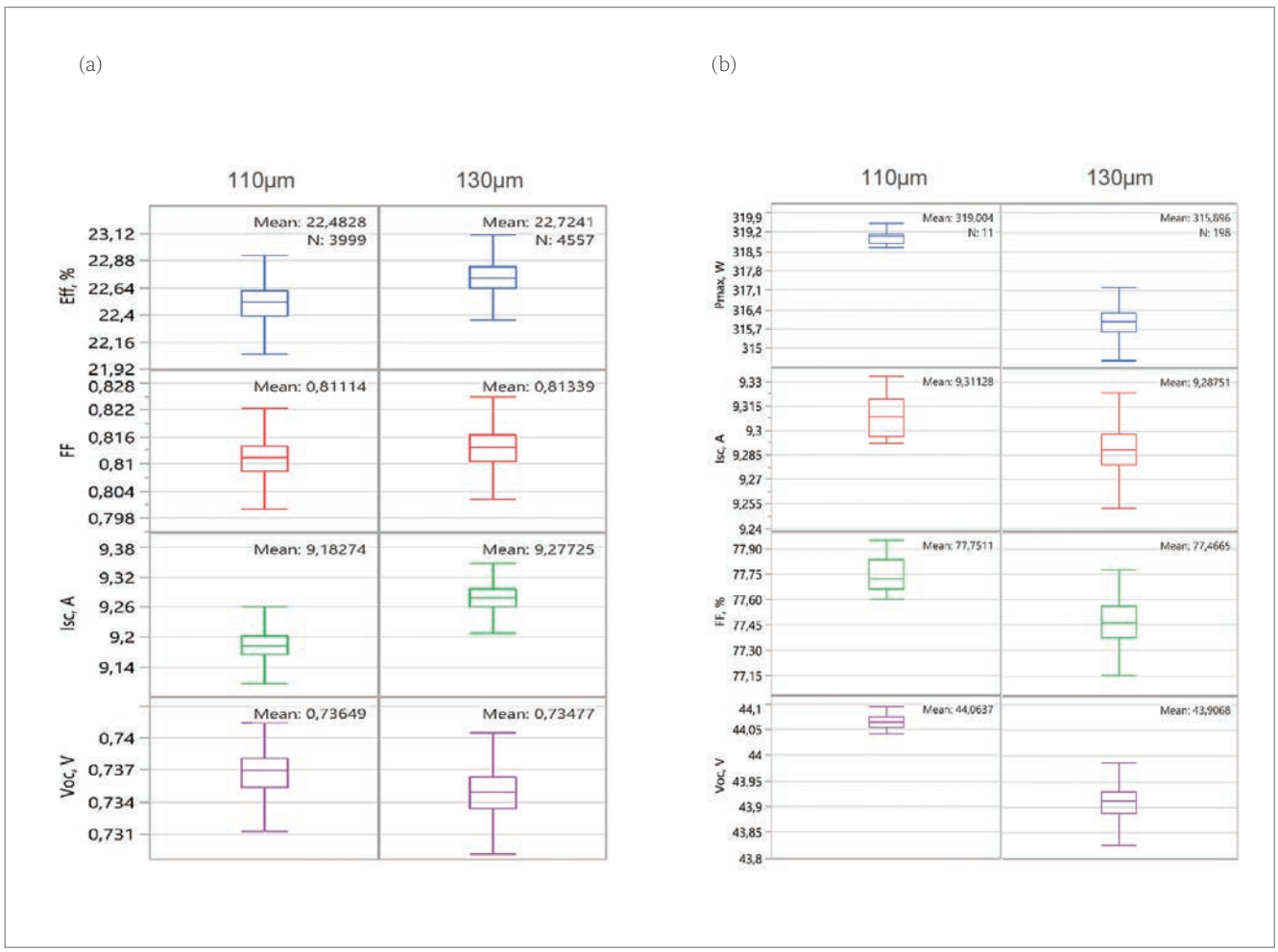

Figure 1. (a) Comparison of the electrical parameters of the HJT cells with thicknesses of ~110 and 130µm, fabricated from wafers with initial as-cut thicknesses of 130 and 150µm, respectively. (b) Comparison of the electrical parameters of the HJT modules assembled from the respective cells. (Note that the results present the state of production in early 2018 and are not representative of the current production level, which is at 23.5 % cell efficiency for 150µm wafers.)

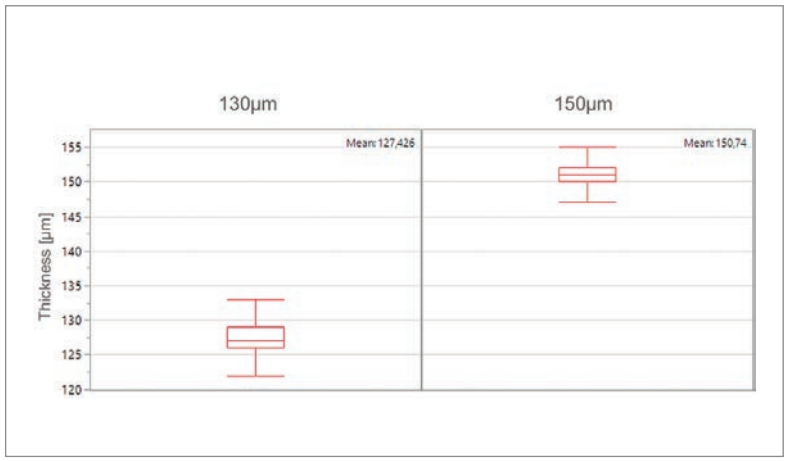

Figure 2. Distribution of the initial n-type c-Si wafer thicknesses used in the HJT production process in this study. The chemical SDE process will further reduce the final cell thickness by approximately 15µm on average, to 115 and 135µm, respectively.

"Wafer handling at all production steps and the thermal stress induced by cell processing are considered the main reasons for cell breakage during manufacturing."

and much lower processing temperatures than other c-Si technologies, the implementation of thinner and larger crystalline silicon wafers is consequently more favourable for HJT. In practice, however, the implementation of thin wafers requires an assessment of mechanical stability and breakage rate, both of which can only be quantified in actual full-scale production.

Earlier manufacturing tests with thin wafers in a pilot-line production [11] demonstrated that HJT cells with initial wafer thicknesses down to 120µm could be processed using existing automatic wafer-handling systems without dramatically affecting the breakage rate and production yield. Further thickness reduction, however, required manual wafer handling and was therefore not suitable for production. During Hevel's full transition to 150µm c-Si wafers in production in 2018 [9], in general no significant breakage or yield reduction occurred; when the initial wafer thickness was reduced from 180 to 150µm, no major modification to wafer handling and transport systems were necessary. Currently, other HJT cell manufacturers use wafers with initial thicknesses in the range 150 to 170µm [12,13].

In the present study, cell breakage rates were evaluated for initial wafer thicknesses of 150 and 130µm (Fig. 2) for individual HJT processing steps separately, as well as for the loading/unloading and cell-handling steps in a full production environment without modifications of production or handling tools. Wet-chemical saw-damage etching (SDE) and texturing treatment result in a further reduction in thickness by approximately 15µm, and so the final cell thickness decreases to 135 and 115µm on average, respectively.

The breakage rates are presented in Table 1. An analysis of a regular production process with 150µm wafers, averaged over many months and many millions of cells, reveals that the most sensitive step with regard to cell breakage in the Hevel production line is the wafer transport and loading/unloading step, while all other steps together result in a similar breakage rate. Among the latter steps, the highest breakage rate is observed during the metallization step, which is performed by standard screen printing.

A reduction of the c-Si wafer thickness to 130µm, corresponding to final cell thicknesses in the range 110–120µm, increases the breakage rates by a factor of two for wafer handling at the plasma-enhanced chemical vapour deposition (PECVD) step, and by a factor of 1.5–2 at the metallization step, while breakage rates at other steps are virtually unaffected. Nevertheless, the total breakage loss values remain relatively low and do not exceed 0.5% for cells fabricated from 130µm wafers, which leads one to believe that with some modification of the wafer handling system, the breakage rate can be kept under control in production, even for such low wafer thicknesses.

One option for reducing the influence of transport on the cell mechanics during HJT processing is to implement contactless cell-handling systems [14]. At the same time, the screen-printing process should be improved in

Process step	150µm wafer	130µm wafer
Wafer inspection (WIS), including chipped wafers	Breakage and chips 0.03%	0.04%
Wet chemistry	0.01%	0.01% Occasional wafer sticking
Loading/unloading and PECVD	0.1%	0.2%
Physical vapour deposition (PVD)	0.02%	0.02%
Metallization (screen printing)	0.04–0.06%	0.08%
Cell inspection	Breakage and chips 0.02–0.08%	Breakage and chips 0.02–0.08%
Total:	0.22–0.30%	0.37–0.43%

Table 1. Breakage rates for the various HJT production steps and for two different wafer thicknesses of 150 and 130µm. The most critical steps (highlighted by shading) for wafers thinner than 130µm in production are the wafer handling and cell metallization equipment.

Module assembly	GG 72-cell (2.4mm glass)	GG 72-cell (2.4mm glass)	GBS 60-cell (3.2mm glass)	GBS 60-cell (3.2mm glass)
Initial wafer thickness	150µm	130µm	150µm	130µm
Wafer size and format	156×156, full	156×156, full	156×156, full	156×156, full
Interconnection type	ECA, 5 busbars	ECA, 5 busbars	SWCT, 18 wires, Ø 250µm	SWCT, 18 wires, Ø 250µm
Cell breakage rate at interconnection step	0.06%	0.06–0.09%	0.11%	0.2%

Note: GG and GBS represent glass–glass and glass–backsheet module types, respectively.

Table 2. HJT module assemblies used in this study and the cell breakage rates detected at the cell interconnection step for two interconnection techniques (ECA and SWCT) and for two different HJT wafer thicknesses of 150 and 130µm.

order to facilitate further reduction of the cell thickness in production. Besides an advanced screen-printing process, recently proposed contactless printing processes – such as pattern transfer printing [15] or multi-nozzle dispensing [16] – should be considered as alternative solutions for forming the metallization grid on very thin cells.

Interconnection process and module assembly

HJT cells require a low-temperature interconnection process that can be performed via soldering [17], gluing by means of electrically conductive adhesive (ECA) [18,19], SmartWire Interconnection Technology (SWCT) [20], shingling or other techniques. In any case, because of the sensitive cell passivation of a-Si:H, the temperature of the interconnection process is limited to less than 200–240°C. It should be noted that the mechanical stability of the interconnected cells in a module is highly dependent on the properties and type of the interconnection materials, primarily the wire or busbar ribbon thickness, the laminate thickness and so on.

In this study, HJT modules were assembled by means of ECA and SWCT interconnections at Hevel's current production facility. Fully automated equipment was utilized for stringing, busing and other module assembly steps. Table 2 presents the details of the module assemblies. Full cell 156×156mm wafers (M2) were used, along with the two different wafer thicknesses of 150 and 130µm (see above). The former is the current c-Si wafer thickness production standard at Hevel, while the latter is used only for assembling a limited number of modules (~20 per module type) as an initial trial. Glass–glass (GG) and glass–backsheet (GBS) module types were produced in order to assess a broader range of products for thinner cells. Fig. 3 shows examples of the electroluminescence images of the finished modules assembled from thin HJT cells.

The HJT cell breakage rates for the interconnection processes are given in Table 2. For standard 150µm cells, ECA interconnection results in slightly lower cell breakage rates than SWCT interconnection; at the same time, both values remain reasonably low. A reduction of the wafer thickness to 130µm results in much higher breakages for SWCT than for ECA. For SWCT interconnection, the number of thin cell cracks rises by a factor of two, while for ECA it still remains at an acceptable level. Apparently, while the SWCT interconnection allows 150µm wafers, a further thickness reduction will require major modifications to the stringer to allow very thin cells in production. The data therefore highlight the fact that the cell interconnection technology is a crucial step which potentially hinders the use of very thin (<120µm) HJT cells in module production. In particular, it is interesting to postulate whether

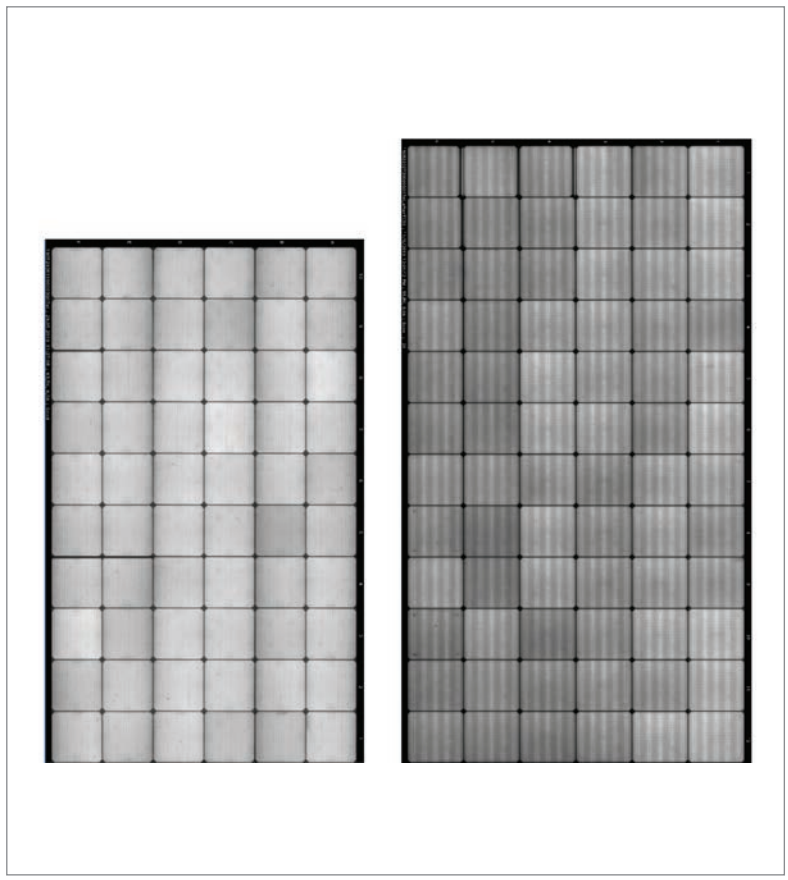

Figure 3. Electroluminescence images of the GBS SWCT-interconnected and GG ECA-interconnected modules assembled from HJT cells with an initial wafer thickness of 130µm.

a multi-busbar (MBB) cell interconnection scheme that is becoming mainstream nowadays will pose similar constraints on the cell thickness to those for SWCT.

HJT module reliability

Cell cracks are one of the most important degradation factors associated with solar modules, especially when thinner cells are considered. Microcracks and chips appearing at different production steps are found to be the main cause of cracks, which can start to propagate over the cell area when thermal or mechanical in-plane tensile stress is induced during module operation. Tensile stress in the cell within a module is strongly influenced by the respective bill of materials (BoM) – glass or backsheet protection cover, interconnection type and wire (busbar ribbon) diameter (thickness), lamination foil thickness, frame design, etc. – as well as by external climatic stress factors.

Several HJT module types (see Table 2) were assembled for laboratory testing with a particular emphasis on cell mechanical stability. As well as the regular tests performed in accordance with the IEC 61215 standard, such as static mechanical load (SML) and climatic (thermocycling/TC, damp heat/DH) tests, extended climatic stress sequences were conducted. These extended tests form part of the forthcoming IEC 63209 standard series – 'Extended stress testing'. In addition, a combined mechanical and climatic stress sequence (SML→DML→TC50→HF10, where DML = dynamical mechanical load), as implemented by several quality programmes other than IEC (e.g. PVEL [21]), was applied. The combined test sequence is believed to be better at reproducing the influence of the interconnection on the mechanical strength of the cells.

Glass–glass (GG) modules were tested in a 72-full cell format and with two different glass thicknesses of 2.4 and 2.0mm; the latter is becoming the mainstream GG product for many module manufacturers. In addition, a 60-cell glass–backsheet (GBS) module was tested. With regard to cell thickness, two different cell types were used, fabricated from 150 and 130µm initial c-Si wafer thicknesses.

GG HJT modules were noted to exhibit excellent mechanical stability of the HJT cells

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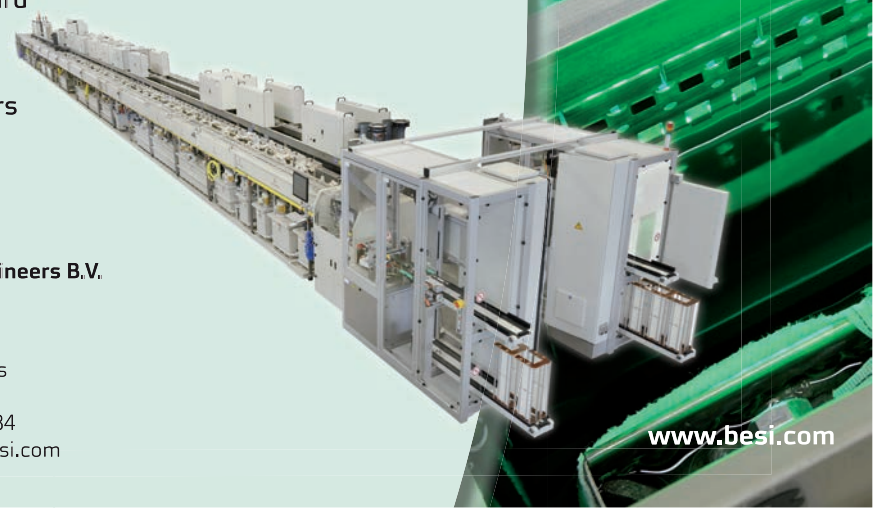

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inside. Indeed, the static mechanical load test performed on many GG modules resulted in zero cell cracks, independently of the cell thickness (150 or 130µm) and glass thickness (2.4 and 2.0mm) used. Generally, the power loss for the GG module after the SML test was well below 1%. Subsequently adding dynamic mechanical loading, followed by climatic stress in a sequence SML→DML→TC50→HF10, results in no cell or interconnection damage, and power degradation still keeps well below 1%. This demonstrates that HJT cells with thicknesses in the range 150 to 130µm can be used in glass–glass module designs without affecting their mechanical stability, provided that an appropriate interconnection scheme and BoM are selected. On the other hand, HJT GBS modules assembled from thin HJT cells exhibited occasional cell cracks under static mechanical tests with maximal loads applied, leading to a power loss ranging from 1 to 4%, depending on the number of cells cracks and cell thickness.

The high mechanical stability of the cells in the GG module is generally believed to be due to the symmetric GG module design, which results in the cells located near the neutral plane coinciding with a zero-stress position, as opposed to GBS modules. Subsequent climatic tests, however, do not affect the module power, as seen in Table 3. To conclude, in terms of module assembly and reliability, a reduction of the HJT cell thickness to 150µm is feasible without significantly affecting breakage rate and module reliability. At the same time, a further reduction of the HJT cell thickness, down to 130µm, will strongly favour GG module technology over the GBS option.

Conclusions

In this paper, Hevel's recent activities on implementing thinner c-Si wafers in the production of HJT solar cells were reviewed. The results demonstrate that the wafer thickness can be reduced to 150µm without affecting production yield, increasing breakage rate and sacrificing module reliability for both glass–backsheet and glass–glass HJT module types. A further reduction of initial wafer thickness to 130µm increases the breakage rate by up to a factor of two during some of the production steps.

> "A reduction of the HJT cell thickness to 150µm is feasible without significantly affecting breakage rate and module reliability."

The most sensitive steps are the wafer and cell precursor handling and the metallization process. Consequently, new or modified approaches to wafer handling that minimize the impact on the cells are required, one of them being contactless wafer transport, for example. The most crucial process that limits the use of very thin (<130µm) wafers in HJT module production is cell interconnection. While it was shown that ECA-type interconnection appears to be the least damaging in the assembly of high-quality modules, the breakage rate could still be minimized by modifying the existing process.

Finally, it was shown that, in terms of module reliability, very thin cells are best assembled in a glass–glass module type, which allows protection of the cells from cracking under different climatic stress factors. To conclude, it is believed that a c-Si wafer thickness reduction to at least 130µm should be possible for an industrial HJT process, provided that the modifications in production equipment are thought through and implemented. As monocrystalline silicon is the most energy-consuming step in the PV module production chain, the use of thinner wafers gives the HJT process a clear advantage with respect to other Si crystalline technologies in terms of lower levels of greenhouse gas emissions.

Module assembly/ Test sequence	GG 72-cell (2.4mm glass)	GG 72-cell (2.0mm glass)	GBS 60-cell (3.2mm glass)	GBS 60-cell (3.2mm glass)
Wafer thickness [µm]	130/150	150	150	130
SML (load: 5,400/2,400Pa)	0.2% No cell cracks	0.2% No cell cracks	1–2% Occasional cell cracks	1–4% Frequent cell cracks
Mechanical stress sequence in accordance with PVEL (SML→DML→TC50→HF10)	0.6% No cell cracks	0.6% No cell cracks	1.3% No new cracks after climatic tests	2–4% No new cracks after climatic tests
TC600	<1.5%	<1.5%	≈2%	≈2%
DH2000	≈0%	≈0%	≈2%	≈2%

Note: SML = static mechanical load, DML = dynamic mechanical load, TC50 = 50 thermocycles, HF10 = 10 humidity–freeze cycles, TC600 = 600 thermocycles, DH2000 = damp heat for 2,000h.

Table 3. Results of reliability tests for the HJT modules with cells of different thicknesses and for different module types. The degradation is shown in % of initial power for individual or sequential tests. The individual tests are performed in accordance with IEC 61215.

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"The use of thinner wafers gives the HJT process a clear advantage with respect to other Si crystalline technologies in terms of lower levels of greenhouse gas emissions."

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When heterojunction meets shingle: R&D activities at CEA-INES

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Abstract

The recent announcements along with the latest very high-power modules reported by the various leading manufacturers clearly indicate that the requirements for module production are rapidly shifting towards new standards, where many new concepts are beginning to emerge. Among these techniques, 'zero-gap', paving and shingling integration in particular are attracting a lot of attention, as they can combine very high efficiencies with improved aesthetics, which are necessary for many PV applications, such as rooftop integration or more general building-integrated PV (BIPV) and vehicle-integrated PV (VIPV). In addition to this denser integration scheme, the incorporation of a 'cut cell' is becoming the norm, because with the increase in both cell efficiency and wafer size (the shift from M2 to M6 and even to M12), it is essential to limit the resistive losses linked to the very high currents generated by such devices. Commercial modules in such configurations are already available, but these are mostly built with technology based on the passivated emitter and rear cell (PERC) concept. Indeed, high open-circuit voltage (V_{oc}) cell configurations, and especially heterojunction (SHJ) architectures, may not appear at first sight to be the most suited to shingling, as performance losses can be fairly significant with the unpassivated edges generated during the cutting step. But, on the other hand, SHJ technology already benefits naturally from the extensive know-how acquired when combining electrically conductive adhesive (ECA) with transparent conductive oxide (TCO) and low-temperature metal pastes. Furthermore, the cell-to-cell overlap significantly decreases the impact of cut-edge defects, thereby minimizing the effective efficiency losses. This paper will accordingly outline the recent activities at CEA-INES concerning the development and understanding of the integration of such shingle cells. The initial focus will be on the impact of the cutting step on final cell characteristics, highlighting the outcomes and challenges related to this critical process step. The main achievements in interconnection and module integration will then be described, with specifically the fabrication of ~400W solar panels featuring high reliability.

Introduction

On the one hand, there is the silicon heterojunction (SHJ) device, which is one of the most attractive technologies, combining high power and a simple fabrication process flow (Fig. 1(a)). Efficiencies greater than 25% on large-area devices have been demonstrated by several companies/institutes [1–3], including recent announcements from CEA-INES [4], proving that the transfer from lab-scale to high production volume is currently accelerating. However, SHJ has also recently faced new challenges, as the module integration scheme is progressively moving towards half-cell or even shingle interconnection. Indeed, as presented in previous publications [5,6], noticeably severe performance losses are observed when SHJ cells are cut, linked to the creation of an unpassivated edge. Several investigative studies on cut optimization or edge repassivation have been conducted, but, so far, most institutes/companies have reported final cell efficiencies lower than the initial full-cell performances [7,8].

"Noticeably severe performance losses are observed when SHJ cells are cut, linked to the creation of an unpassivated edge."

On the other hand, there is the shingle interconnection scheme, which is quite an old concept (first patented in 1956 – see Fig. 1(b)), but currently regaining more and more interest, as it combines several advantages and appears to be particularly adaptable to new PV challenges. In fact, with the increased active area linked to the tile overlap, and the low electrical resistance of the assembled interconnection, very high-power densities are achievable [9]. Furthermore, because of the formed uninterrupted silicon array, and the absence of interconnection wires or ribbons, the global aesthetics are significantly improved, thus meeting the new demands and requirements for large-scale deployment in building and vehicle applications.

But what happens when SHJ and shingle concepts are combined? Certainly, the consequences of moving towards this new module design must be properly evaluated, not only in terms of module final performance but also in terms of long-term module stability and reliability. Such analysis has already been initiated by Gérenton et al. [10] for half-cell configurations, but even stricter constraints can become apparent when a shingle interconnection is considered. As shown in Harrison et al. [6], up to $1\%_{abs}$ efficiency losses can be observed after cutting an SHJ cell in a thin shingle stripe configuration. These losses, however, are expected to be reduced after module integration, since no carriers will be generated next to one of the defective edges thanks to the shading created by the natural cell overlap that occurs in shingle integration. Furthermore, the need for ECA in shingle interconnection seems particularly well suited to an SHJ configuration, as the interactions of this type of conductive paste with ITO and low-temperature paste have already

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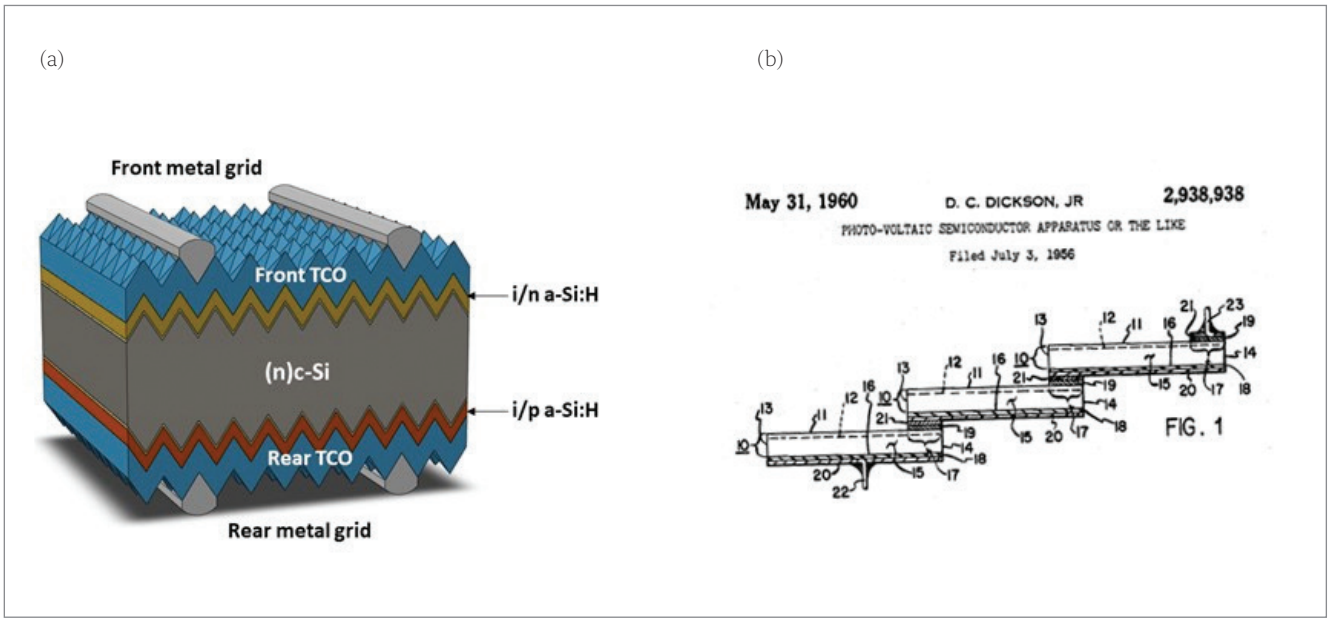

Figure 1. (a) Schematic of the heterojunction cell device used. (b) Picture taken from a 1960 patent, already describing the shingle concept in use today.

been widely studied, especially for traditional ribbon attachment [11].

This paper will first introduce the specific constraints and achievements with regard to the SHJ shingle cell, before presenting the development work conducted using the CEA-INES production line. Finally, major interconnection and module results will be detailed, with in particular the fabrication of the first large-area device (equivalent to 72 cells), for which promising power and reliability results have already been demonstrated.

Shingle SHJ cells

The core process of the SHJ shingle cells remains unchanged, meaning that all texturization, cleaning and deposition steps are identical to standard production processes [12]. However, if the metallization step still relies on screen-printing for the paste transfer, it will need to be adjusted to the specific shingle configuration. Indeed, for shingle cells, the busbar is relegated to the edge of each tile; while this imposes an interrupted finger design, as described in Fig. 2, it also leads to very effective longer metal lines, twice the length they would otherwise be in a conventional centred six-busbar design.

As the metal paste conductivity is limited by the heterojunction temperature constraints, a double-print process is introduced for the front side [13], allowing a good compromise to be achieved between overall finger optical shading and high cell performance. On the back side, in contrast, a simple print process is retained, as the dense grid pattern used for standard cells is sufficient for limiting the parasitic resistance. The paste consumption increase, when compared with standard SHJ devices, remains thus limited, even

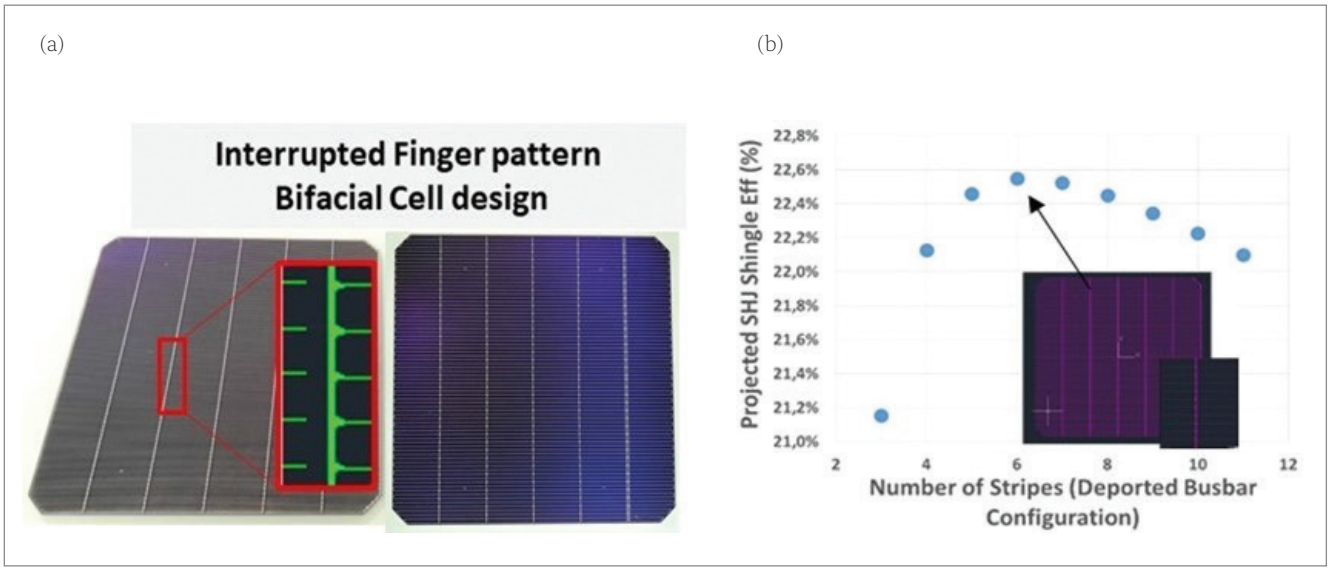

Figure 2. (a) Photo of a fabricated SHJ shingle cell, with a schematic of the specific busbar and interrupted finger design. (b) Optimization of SHJ shingle tile length, to reach a compromise between metal resistance and cut-edge impact.

Figure 3. CEA-INES heterojunction production line. All the shingle cells were manufactured on this industrial platform.

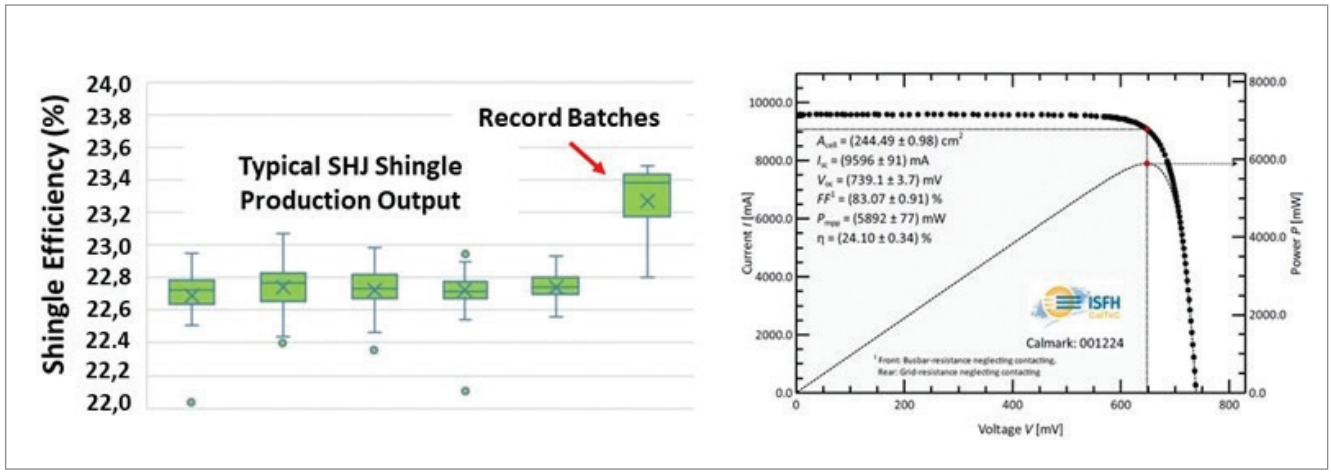

Figure 4. (a) Typical efficiencies obtained with SHJ shingle cells on the CEA-INES production line. (b) Record shingle cell certified @ 24.1%.

"A six-stripe configuration (26mm tile length, M2 size wafers) appears to be the optimum choice for a satisfactory compromise between cut-edge impact and global metal resistance."

if further developments or alternative metallization schemes [14,15] might be beneficial to improve the competitiveness of such cells.

Small length tiles could therefore be interesting for SHJ, but to define the optimum tile length, it is also necessary to take into account the losses in efficiency after the cut. As will be described in the next section, the performance can be significantly degraded if tile dimensions that are too small are considered. Finally, a six-stripe configuration (26mm tile length, M2 size wafers) appears to be the optimum choice for a satisfactory compromise between cut-edge impact and global metal resistance. Such a tile length is still fully compatible with industrial constraints, and suitable with regard to current stringer constraints. Finally, it is worth noting that the shingle cell design remains highly bifacial (>85%), and can still benefit from the power increase linked to illumination albedo, with this being taking into account, if possible, during the system installation.

Solar cell batches – compatibility with high-efficiency requirements

Shingle cells used in this study were all produced on the CEA-INES industrial 'LabFab' platform (Fig. 3), as described in the previous section. Thousands of cells (>4,000 cells) were fabricated, with typical average efficiencies measured in the 22.6–22.8% range (Fig. 4(a)), illustrating the perfect compatibility of the adapted process to a standard production line. It is worth mentioning that, with simple process improvements and diminished throughput, record batches with up to 23.4% efficiencies were obtained, demonstrating the possibility of achieving very high efficiencies with this technology. The record cell was certified at 24.1% (full M2 size), although the production process included an additional technological step that was not fully compatible with current high-throughput constraints (Fig. 4(b)). This excellent result demonstrates, however, that there is potential margin for optimization, and that the SHJ shingle configuration is fully consistent with high-performance needs.

Cutting step impact

Cutting is the most critical process step for shingle heterojunction devices. Indeed, the high bulk quality, coupled with the absence of a strong internal field effect and the very high passivation levels reached for the SHJ architecture, leads to very high sensitivity of the structure to the edge defects generated during the cutting step [16,17]. Simulation studies even show that the edge defect impact can extend up to 3mm inside the bulk, thus greatly affecting the charge recombination and the final fill factor (*FF*) achievable [18]. In a half-cell configuration, up to

0.3%$_{abs}$ efficiency losses are generally measured after separation. For shingle tiles, the situation is even worse: because of the lower surface to perimeter ratio, and the creation of two defective edges, up to 1%$_{abs}$ losses can be observed on the final devices (Fig. 5).

Such a high level of edge defectiveness is thus clearly a critical limiting factor, and many development studies have been initiated in order to optimize and better understand how to limit the associated performance losses. For heterojunction devices, it is mandatory to limit as much as possible the parasitic heating that occurs during the separation process; for traditional laser-cutting approaches, this translates into only partial silicon ablation (typically, it is necessary to target a scribe length of one-third of the initial wafer thickness), followed by mechanical breakage. Several laser passes are considered for the ablation step to limit the heating. Despite the precautions taken, however, both active layers and silicon bulk volume show fairly significant morphology degradation around the newly created open edge [8]. Consequently, alternative cutting techniques have also been evaluated. It is worth mentioning in particular the thermal laser separation (TLS) approach [19,20], developed by the company 3DMicromac, as well as an innovative integration proposed by CEA and relying on 45°-rotated ingots [21]. The TLS concept relies essentially on thermal mismatch for the crack propagation, while the 45° ingot concept takes advantage of the natural privileged (110) crystalline fracture line that is thus now aligned with the desired cut lines, allowing a full mechanical separation process.

Nevertheless, as shown in Fig. 6, the final efficiency losses all remain very similar, measured again in the 0.25–0.3%$_{abs}$ loss range. This highlights that if the cutting process (in particular the laser-based scribing) is properly optimized, the damage inflicted upon the SHJ device remains limited, and the main losses observed are essentially linked to the extremely high impact of the generated unpassivated edges. This finding is particularly true for SHJ architectures, again because of the very high carrier lifetimes observed in such devices, but will probably apply to all alternative architectures, such as tunnel oxide passivated contact (TopCON) or poly-Si-based structures, whose passivation levels are also reaching very high levels.

A comparison of the three cutting techniques shows clearly very different cut-edge morphologies, with very smooth surfaces obtained for both the TLS and the 45° ingot approaches. This morphological improvement is essential for two major reasons. First, the likely reduction in local micro-cracks will help to lower the overall breakage rate when module production is considered. Second, as mentioned previously, edge repassivation might be mandatory in order to mitigate the observed losses and recover performance; all research activities published so far, however, show that such processes are not compatible with laser-based scribing methods [6,7,22].

Cut-edge defectiveness: how to moderate its impact?

It would not be appropriate to go into too much detail in this overview, as much R&D activity is currently still ongoing, and the current assumptions and findings may rapidly change over the

"The main losses observed are essentially linked to the extremely high impact of the generated unpassivated edges."

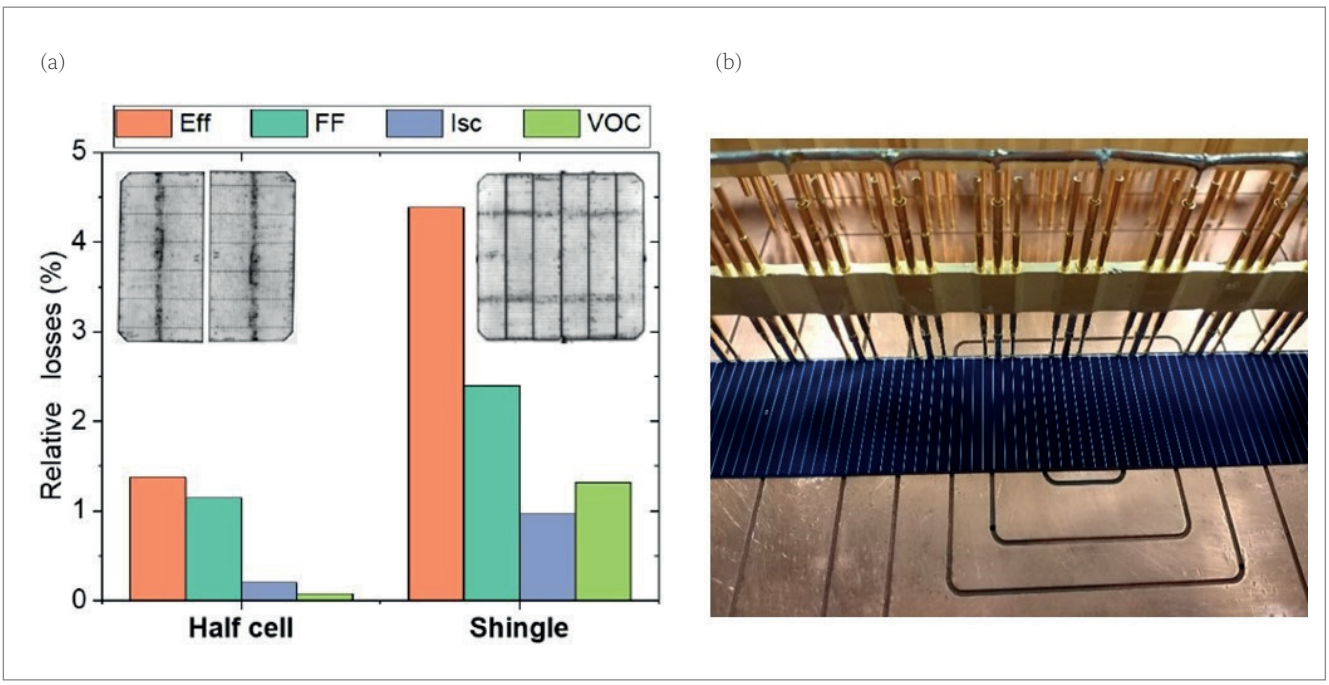

Figure 5. (a) Typical efficiency losses measured after cell separation for half-cell and shingle configurations. (b) The measurement set-up for an isolated shingle tile.

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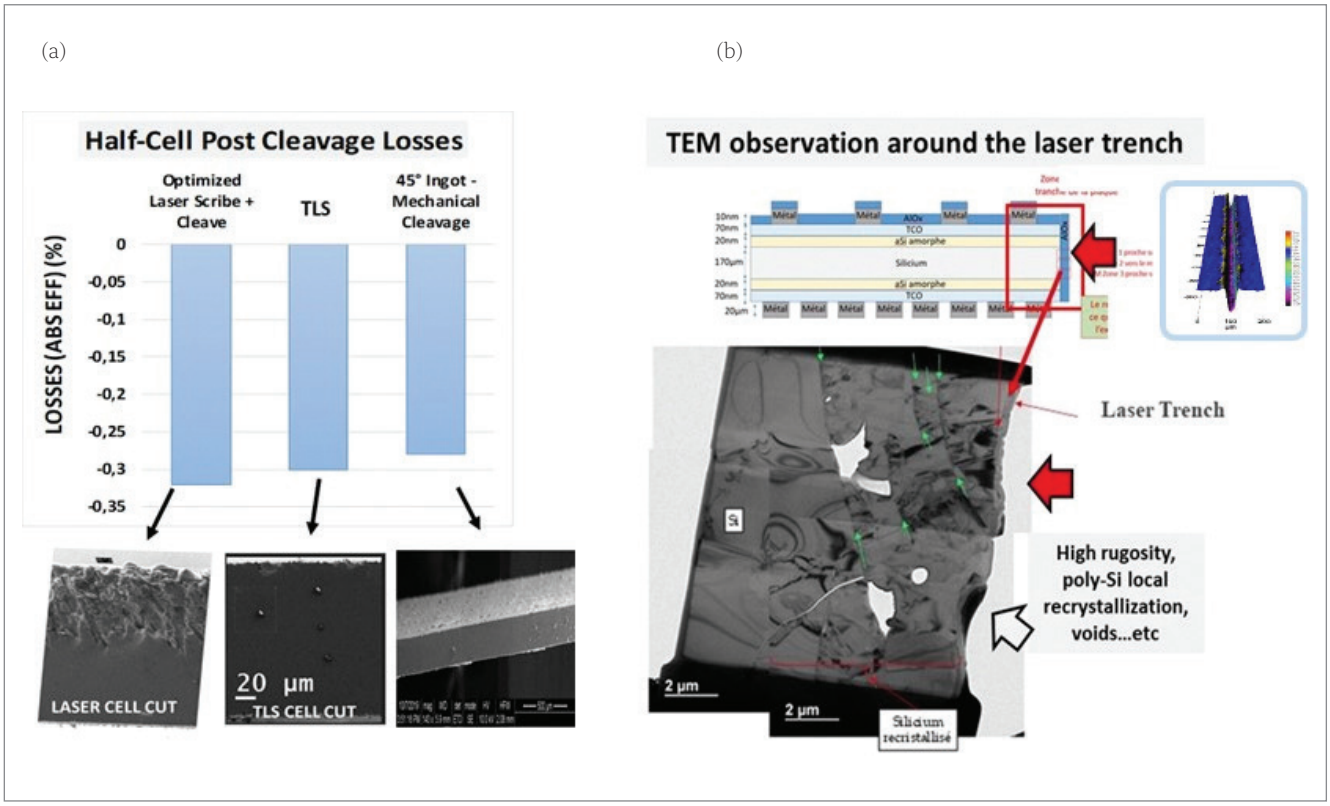

Figure 6. (a) Comparison of different cutting techniques. If very similar performance losses are observed, the final cut-edge morphology shows a smooth appearance for the TLS and 45° ingot approaches. (b) Strong degradation of both active layers and silicon bulk around the laser trench is confirmed by local transmission electron microscopy (TEM) observations.

coming months with the expected technological improvements and the rapid emergence of innovative solutions. However, it would be useful to mention several activities that could lead, either separately or cumulatively, to a significant reduction in the observed apparent losses due to cutting.

First, it is worth pointing out that, because of the specific shingle configuration, a natural cell-to-cell overlap occurs, meaning that one of the defective edges is shadowed by the adjacent integrated tile. This is important, since free carriers are therefore generated further away from the cut-edge, thus minimizing its true impact when integrated in the final module. This is illustrated by the *I–V* measurements shown in Fig. 7, in which an *FF* gain, for example, can be clearly seen when the masked edge length is progressively increased. However, this cell-to-cell overlap increase must remain limited when the final product is considered, as a compromise between performance

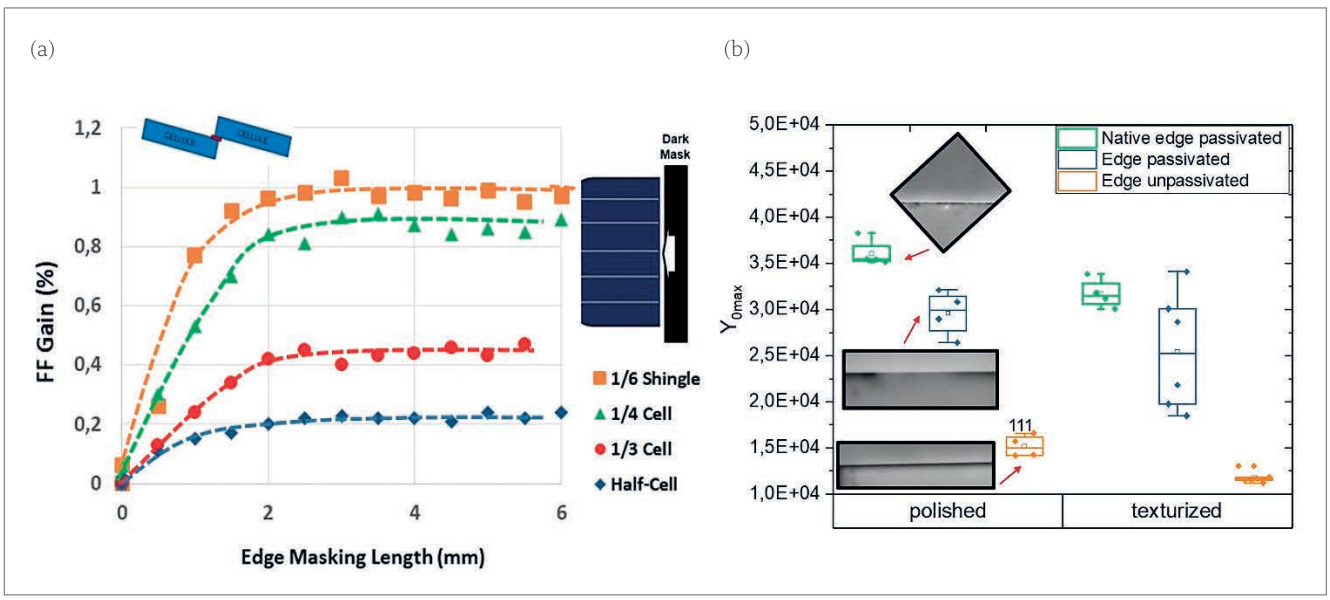

Figure 7. Illustration of paths of improvement for minimizing the impact of edge defectiveness. (a) Improvement that happens naturally, thanks to the cell-to-cell overlap. Significant performance recovery can be realized with a moderate overlap of, for example, 1mm. (b) Additional process steps, dedicated to edge passivation might be necessary to further improve the module power. This graph shows that the local deposition of amorphous silicon allows a distinct recovery of lost performance (Y_o metric based on PL edge signal extraction; high values of Y_o represents high passivation values).

Figure 8. BSC SONETTO stringer developed by Amat-Baccini, with additional images of the strings produced, as well as of the typical stripes obtained after the cutting of the cell.

recovery, final product power and overall cost might need to be found.

With regard to the edge passivation approach, many ideas are being tested [7,8,23,24], but no clear technological solution has emerged yet. The topic is indeed quite complex for SHJ, mainly because of the temperature constraints; the importance of hydrogenation and the need for very clean and smooth edge morphology both appear to be critical in order to reach locally the necessary high passivation levels to improve the performance of the cut cell. However, the initial results obtained, mostly with the deposition of appropriate layers on the cell edge (amorphous silicon, AlO_x or SiN_x, for example), demonstrate that promising improvement paths are certainly possible, even if only partial recovery has so far been achieved in internal investigations [6,25].

Alternative optimization paths (not mentioned in this article) can also be considered, with in situ passivation during the cutting step, the use of organics or polymers for the edge passivation, and an optimization of the cell integration process (for example, the use of low-resistivity wafers, or an optimization of TCO edge exclusion). In all cases, the implications of additional dedicated passivation steps must be properly assessed at the industrialization level, and the impact on both integration complexity and overall product cost needs to be evaluated in some detail.

Interconnection

A completely new interconnection scheme had to be developed for SHJ shingle purposes. ECA is already widely used for conventional ribbon-gluing interconnection, which is one of the most common interconnection approaches developed for standard SHJ modules. Thanks to the extensive know-how acquired when combining ECA with both metal paste and TCO, it was possible to define an adequate metal pattern for shingling in the interconnection area; the cell-to-cell adhesion is optimized, with sufficient contact area between ITO and ECA, while ensuring proper electrical continuity between the metal lines/busbar in contact with the ECA [26]. To limit the ECA consumption, regular pads of ECA are deposited instead of continuous paste deposition.

"A completely new interconnection scheme had to be developed for SHJ shingle purposes."

Interconnection development and string realization were a joint undertaking with the company Amat-Baccini, located near Treviso in Italy. All strings were fabricated on its dedicated BSC SONETTO industrial equipment (Fig. 8), which allows in succession:

1. Cell scribing and mechanical cleaving.
2. Deposition of the ECA on the Ag pads present on the busbars.
3. Alignment of the cut cells, or shingles, to form the string.
4. Attachment of the end ribbons to the string via ECA.
5. Final curing process.

The fully automated equipment adopted for the test is based on:

- A laser platform with a galvanometer scanner.
- A screen-printing system to deposit the ECA, with a typical printing speed of 200–300mm/s.
- Linear motion units to handle the shingles with precision.
- An integrated device to deposit and align the end ribbons to the string.
- A continuous oven capable of performing the curing with a maximum process window of 200°C and 90 seconds.

The equipment was tested at 4,000 wph in a dual-lane configuration.

It was then possible to rapidly assemble several small-dimension strings to validate the different technical choices made, and to optimize the overall process. This preliminary work allowed in particular to confirm the good compatibility of the ECA chosen with the metal design specifics, to optimize the

integration conditions (pressure, curing temperatures, etc.), and to build the first mini-module. This mini-module was submitted without delay to the usual ageing tests (thermal cycling – TC – in particular, which is the most critical for the shingle configuration). The TC tests revealed excellent reliability, with power losses less than 2% observed after up to 800 TC cycles (Fig. 9); this is an excellent result, confirming the perfect match between SHJ architecture and shingle interconnection [27].

Further experiments were subsequently conducted to further optimize the stringing. It was possible to validate that the developed process remains fully reliable with a significant reduction in ECA consumption, dropping from ~20mg to ~12mg per cell (only 2mg per tile!), which represents almost a 50% material saving without power or reliability degradation.

Similarly, it was proposed to evaluate whether using thinner wafers, down to a thickness of 120µm (which is expected to soon become the norm), could affect the defined interconnection scheme. Again, very good output power values were achieved at the mini-module level (equivalent to a two-cell configuration), with excellent reliability. The breakage rate remained unchanged, despite the thinner material used, and very limited process modifications were necessary – essentially during the final curing step to avoid excessive bowing of the wafers.

Examples, and details of the interconnection trials performed, are presented in Fig. 10, along with microscopic images of the interconnection pads and the ECA used. Following these promising initial sets of results, upscaling of the technology was initiated and the first large-area modules built, as described in the next section. It is worth noting that, even if the process developed is already very satisfactory, a margin for optimization may still be possible. Development work is currently under way to reduce the cell-to-cell overlap down to 0.5mm, or to increase the global throughput of the stringer tool, which could soon demonstrate that even better results might be achieved with SHJ shingle technology.

Upscaling and large-size module integration

The promising results obtained for a mini-module configuration now needed to be successfully transferred to a long-string configuration. A 37-tile configuration was first chosen (string ~1m in length), with a cell-to-cell overlap of 1mm. This length of overlap appears to be a good compromise between active area silicon integration and ease of fabrication, as it allows a comfortable margin in the successive critical alignment steps needed for a proper shingle integration: 1) front and back metallization; 2) ECA with metallization; 3) laser cutting; 4) cell-to-cell automated placement. Furthermore, as illustrated in Fig. 7, it may not be so interesting to switch to more aggressive overlaps, since part of the power gain could be masked by the greater impact of the defective edge. However, experiments to study the impact of a tighter overlap (down to 0.5mm overlap) are already in progress, and preliminary results should be soon available.

"The TC tests revealed excellent reliability, with power losses less than 2% observed after up to 800 TC cycles."

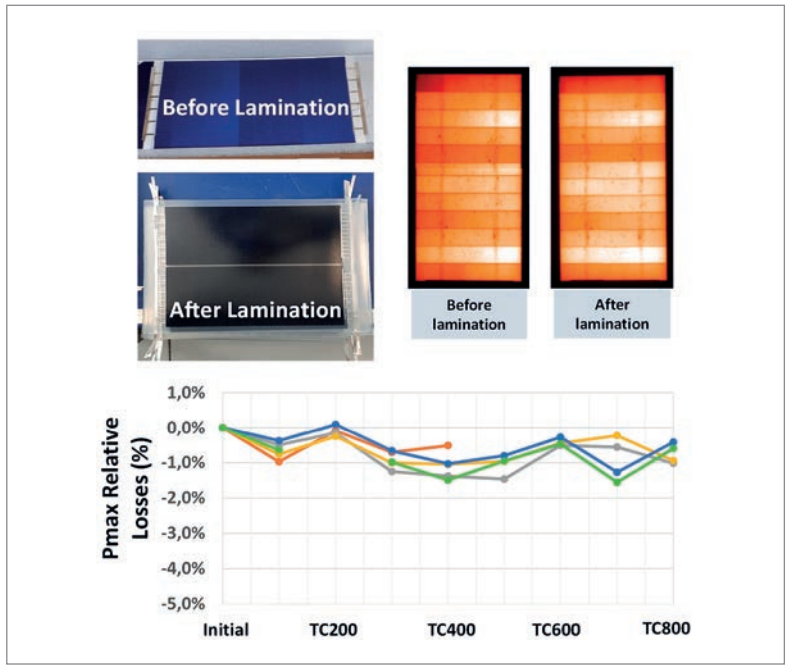

Figure 9. Example of SHJ technology development undertaken at the mini-module level. Outstanding reliability was obtained, and no evidence of cell breakage or degradation was observed during the lamination step.

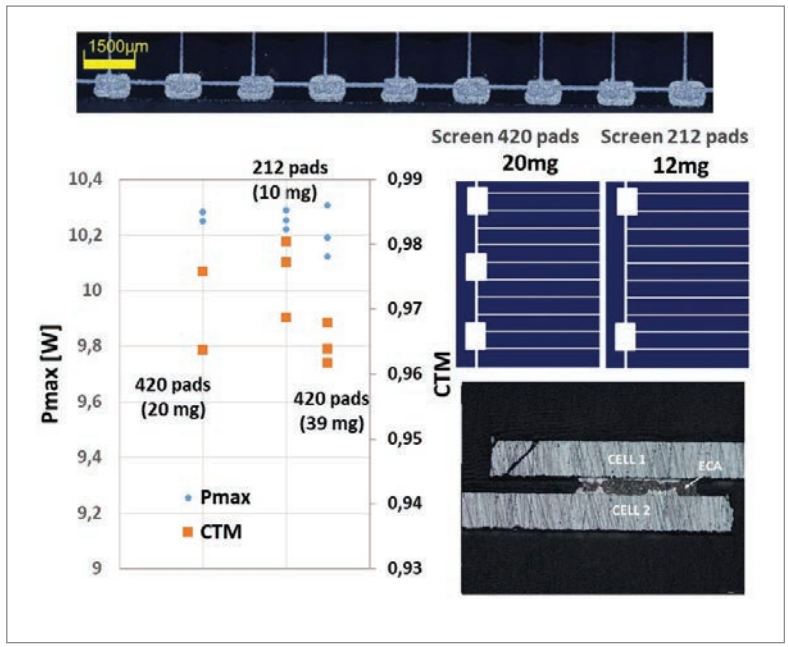

Figure 10. One of the most promising paths of interconnection improvement is the possible reduction of ECA paste consumption. The top image shows a perfect alignment of the ECA with the metal pads used, and the total amount of ECA deposited can easily be reduced either during the printing step or by using a fewer number of metal pads. Excellent power and cell-to-module (CTM) ratio results are obtained (bottom images), even with a minimal usage of ECA (12mg for six tiles, equating to just 2mg per tile). The reliability also remains excellent (not shown here).

Despite only 200 TC having been completed at the time of writing, the initial ageing tests conducted on this intermediate module configuration seem to confirm the excellent reliability of the technology, and the greater dimensions of the manufactured strings do not translate to increased fragility during manipulation or lamination [27]. As shown in Fig. 11, very similar output power and reliability results are again observed with thinner wafers (120μm thick), and the behaviour seen is very close to that of a mature alternative interconnection scheme, such as SmartWire Connection Technology (SWCT).

"Excellent module outputs were achieved, with up to 396W being measured on the module with a semitransparent backsheet."

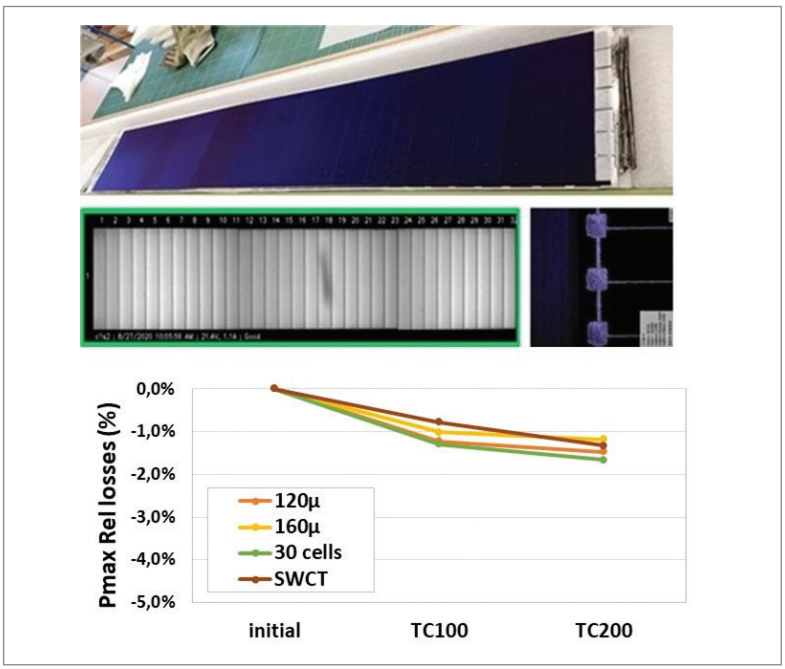

Figure 11. Successful upscaling of SHJ shingle technology. Shingle strings ~1m long were successfully assembled, yielding excellent initial reliability results (200 TC cycles achieved so far).

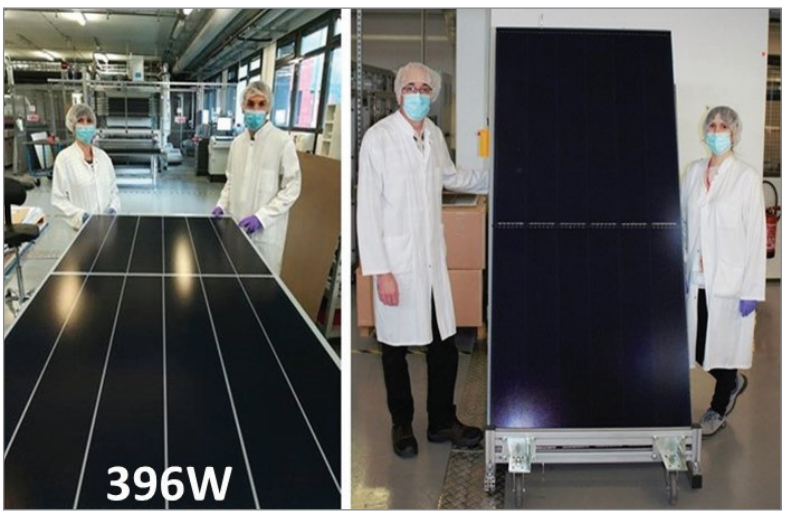

Figure 12. The two fabricated large-area SHJ shingle modules. Close to 400W was measured for the best module, demonstrating the high potential of SHJ shingle technology.

Finally, the first large-area modules were fabricated (Fig. 12) with the interconnection scheme that had been extensively validated by the smaller module configuration [28]. In particular, a cell-to-cell overlap of 1mm was kept, and a total ECA amount of 20mg per cell (six shingle tiles) deposited. Cells with an average efficiency of 22.7% (average production output) were integrated. Further experiments using record batches (average efficiencies of up to 23.4%), however, will be initiated soon, as a higher volume of production is still necessary for large-module considerations.

A standard glass dimension of 2,029×998mm² (equivalent to 72 cells, standard glass) was chosen, even though with this size, the filling of the module with the shingle tiles is still not optimum. The modules were assembled with 12 vertical strings, each integrating 39 SHJ shingle tiles. The first module was integrated with a semitransparent backsheet (85% transparency), with a focus on module performance, reliability and bifaciality. The second module was integrated with a black backsheet, where not only power but also global aesthetics are the priority.

Excellent module outputs were achieved, with up to 396W being measured on the module with a semitransparent backsheet. A module efficiency of 21.6% was calculated when just the active area was considered, as the glass size used was not perfectly adapted to the string length produced. However, with a CTM ratio of 94% (including the cell-cutting losses), and a global bifaciality ratio of 86%, the high potential of combining SHJ and shingle has already been demonstrated. (Although 86% is a satisfactory, considering the semitransparent backsheet, this value will be improved with the use of a glass–glass module configuration). A significant increase in module power output is nevertheless still expected, thanks to a combination of higher cell efficiencies and further optimizations of module integration.

Module optimization: what's next?

Many optimization paths can still be explored for the developed SHJ shingle technology, and even more competitive module powers and costs are probably achievable with limited process adjustment. The edge passivation trials have already been mentioned, but there is also a potential margin for optimization in the metal-interconnection scheme itself.

The simulation tool CTMOD, developed at CEA [29], was used to further examine if an alternative cell metallization compromise was possible, and if a better compromise between silver consumption and performance could be defined. The simulations carried out for a 78-cell-equivalent shingle module (M2 cells cut into six pieces) show, for instance, the impact of the front and the rear metal grid pitch. Finger width is fixed at 70μm, as measured experimentally on standard shingle cells. Regarding the front grid, the optimum pitch was found to be around 1.8mm, even though module performance does not vary very much in the 1.5 to 2.1mm pitch

range (ΔP_{max} < 1.5W). In contrast, modification of the rear grid pitch has a tremendous impact: reducing the pitch from 0.7mm to 0.35mm, for example, allows a power increase of about 5W, but at the cost of double the total silver consumption for the back side (Fig. 13).

Another important topic is the optimization of the cell-to-cell overlap. As mentioned previously, a conservative overlap of 1mm was retained for the shingle experiments presented in this paper. However, moving towards a 0.5mm overlap would allow an important gain in power (almost 10W for a 72-cell-equivalent module, equating to a 2% power increase). But, at the same time, because of this smaller overlap, each constructed string would end up being longer (~19mm longer strings for the 72-cell-equivalent module considered). The longer string dimension would require an increased module size, ultimately leading to a reduction in the final efficiency obtained for such a module configuration (Fig. 14). There are thus different possible compromises possible when the final module configuration is defined, depending on the main driver that needs to be maximized (P_{mpp} or efficiency) for the module application.

Finally, the upscaling of the technology towards long strings or large-area modules was already discussed in the previous section, but what about the upscaling of the wafer size, which is happening today in the PV market? The number of stripes per cell is undoubtedly a compromise between edge-cutting losses and resistive losses linked to the cell metallization. By moving to M12 wafer size, the fact that more cuts are necessary to achieve an optimum module power becomes all the more obvious. The CTMOD simulations did indeed predict that for an M12 cell module, each cell should be cut into seven pieces, for a final width of~30mm for each sub-cell (Fig. 15). If this would be beneficial in decreasing the relative impact of the edge-losses, solutions to improve the metal line resistance would nevertheless still be required.

Conclusion and perspectives

This paper has provided an overview of the different opportunities, but also the challenges, associated with the integration of SHJ technology in a shingle configuration. Indeed, despite many shingle modules being already commercially available, to the authors' knowledge they mostly integrate standard technology, such as PERC devices. Although SHJ technology is naturally well suited to the shingle interconnection, with excellent results having been obtained at both the cell and the module level, optimization is still necessary in order to take full advantage of the very high efficiencies brought about by the use of SHJ.

The performance loss after the cutting step remains high, but several technical solutions for loss recovery are currently under development at the laboratory level. Similarly, metal paste consumption is higher because of the greater length of the metal lines due to the relegated busbar configuration. An alternative metallization solution might need to be considered (for example plating), even if the impact on final cell cost of ownership (CoO) remains limited (Fig. 16). Nevertheless, with a record cell certified at 24.1%, and modules fabricated with power values close to 400W, the high potential of SHJ shingle technology has been demonstrated. With further

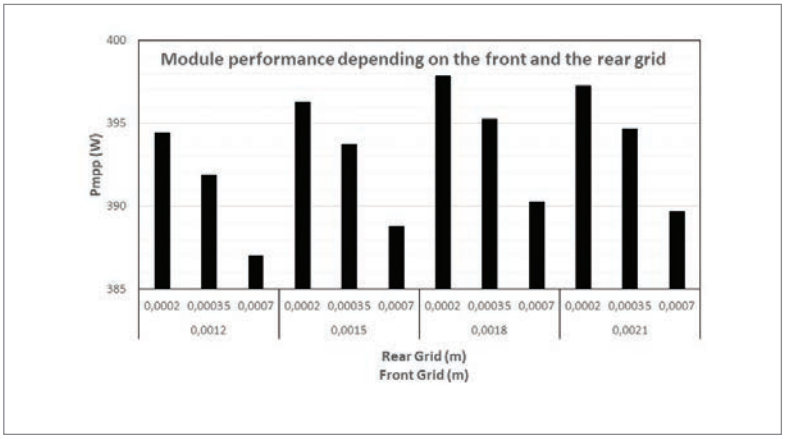

Figure 13. Simulated impact of the front and back cell metal pitch on final SHJ module output power. As shown, a greater margin for optimization (compromise between silver consumption – cost – and module power) can be achieved with a reduction of the back-side metal pitch.

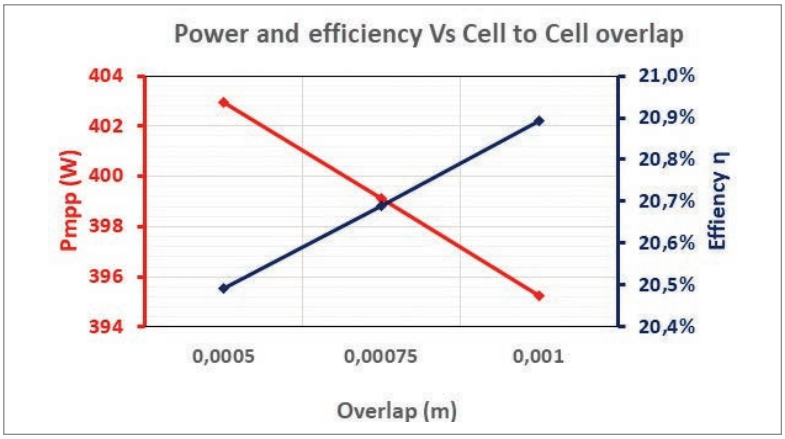

Figure 14. Simulated SHJ shingle module power and efficiency for different cell-to-cell overlaps. Higher power can be obtained with a smaller overlap, but because of the increased final string length, the module dimension needs to be adjusted, ultimately resulting in lower module efficiencies.

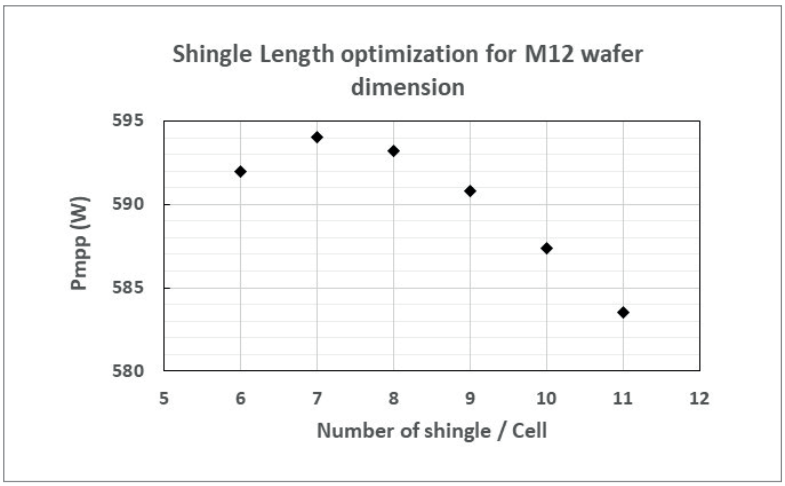

Figure 15. Optimization of SHJ shingle width for M12 wafer size.

"With a record cell certified at 24.1%, and modules fabricated with power values close to 400W, the high potential of SHJ shingle technology has been demonstrated."

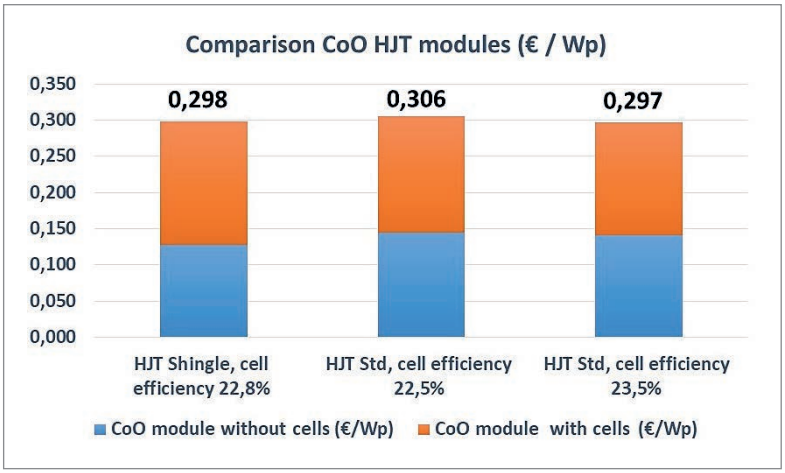

Figure 16. Initial CoO evaluation for SHJ shingle technology. If similar cell efficiencies are considered in order to emphasize just the impact of the bill of materials differences (BOM), shingle technology is shown to remain competitive as the increase in cell cost (linked to the metal cost increase) is compensated at the module level by the reduction in ribbon and ECA consumption. The actual costs are even comparable to those for standard SHJ module integration of higher efficiency cells (up to 23.5% in this calculation).

optimizations and the integration of the fabricated record cell batches, even higher module powers will soon be achieved, paving the way for larger scale exploitation.

Acknowledgement

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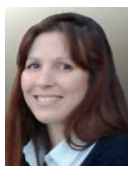
About the Authors

Samuel Harrison obtained his Ph.D. in 2005 in microelectronics, investigating advanced CMOS components, and then worked for Philips Semiconductors on industrial CMOS integration. He joined CEA in 2007, initially involved in microsystems development, before switching to the PV department in 2009. His work has since focused on heterojunction crystalline cells, with a contribution in particular to the ramp-up of the industrial pilot-line, while also leading several research activities on alternative cell concepts.



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IBC technology: Back contacts move to the front

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Abstract

The year 2016 saw the start of the field of PV becoming highly dynamic in terms of the implementation of innovations within solar cell and module production. Since then, Al-BSF devices have been in decline, as more-advanced and higher-efficiency solar cells and modules begin to enter the PV market, achieving the lowest-cost electricity production. The holy grail of every solar cell producer is the creation of a low-cost interdigitated back-contact (IBC) solar cell with an efficiency greater than 25%, a goal that can be found in almost every roadmap presentation. In this paper it will be shown that we are not far away from achieving this target, since IBC devices, with different process complexities, are already in production at several companies. It will be explained why PERC-based IBC processes are the future, not only for rooftop applications but subsequently for the utility-scale market as well. Because of this rapid take-up, FhG ISE, TNO and ISC Konstanz will be reactivating the back-contact workshop in order to bring the whole PV community together again to work on back-contact technology for the PV future.

Introduction

"Solar is the new king of energy markets" is what the International Energy Agency's executive director, Fatih Birol, stated in early 2020 [1]. He said this despite having never been a fan of renewables in previous years, but now he does not have any choice: in some countries (e.g. in the Middle East North African – MENA – states), PV is achieving electricity generation costs well below 2US$¢/kWh, as seen in many offers for energy tenders, including the 800MWp plant planned in Qatar by TOTAL, with 1.567US$¢/kWh [2]. The installation will use bifacial horizontal single-axis tracking (HSAT) with bifacial passivated emitter and rear cell (PERC) modules; this type of system has been attracting a lot of attention in the last two years, since the combination of these technologies leads to the lowest possible levelized cost of electricity (LCOE). In the following discussion, it will be explained why front contacts used to be thick on semi-square cells in the past, are now being printed thinner and thinner on full-cut square cells today, and will eventually completely disappear from the front in the future, as depicted in Fig. 1.

Fig. 2(a) shows the end of a decade of long domination by the very simple aluminium back-surface field (Al-BSF) technology using mostly cheap mc-Si (blue bars in the chart), but also some of the more expensive mono Cz-Si wafers (orange bars).

In 2016 the situation changed dramatically, as LONGi launched low-cost monocrystalline c-Si wafers onto the market, and the PV industry started to become more innovative in terms of implementing new cell concepts, such as PERC and n-type passivated emitter rear totally diffused (nPERT), which had actually already been developed in the laboratory several years earlier. The arrival of low-cost mono wafers also heralded the beginning of a new bifacial era, since good material quality allows a better implementation of an open rear side. It was therefore no great surprise that LONGi became the first Tier 1 company to announce a bright future for bifacial PV in 2017 [4], pushing bifacial PERC onto the PV market. The other large bifacial company, Jolywood, is betting on nPERT

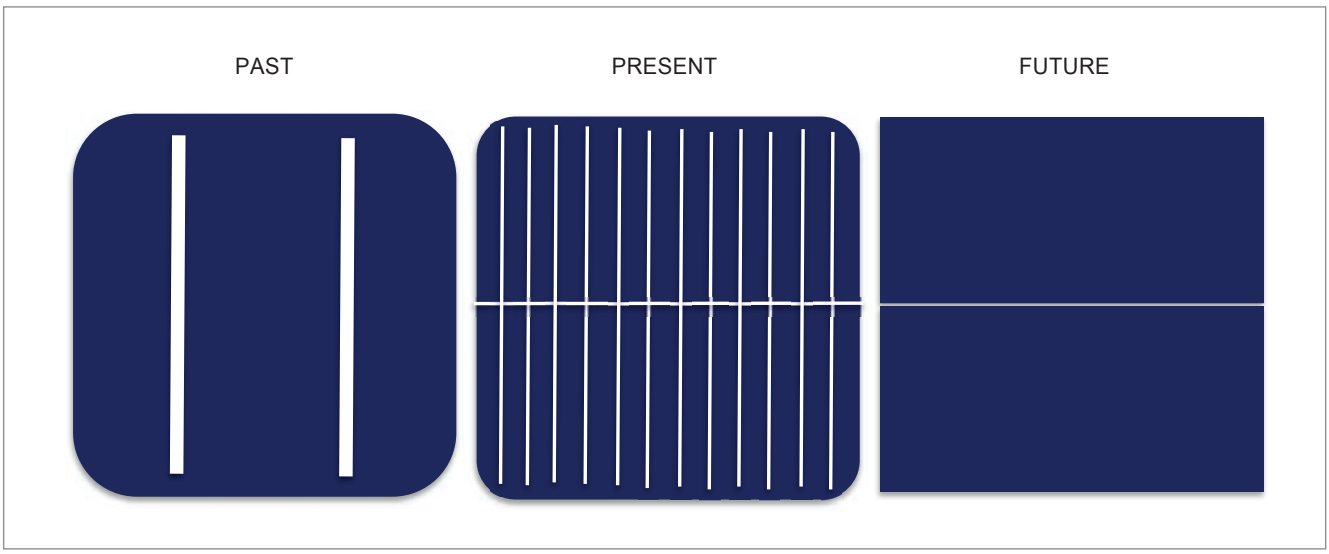

Figure 1. Schematical depiction of the past, present and future of c-Si PV solar cells.

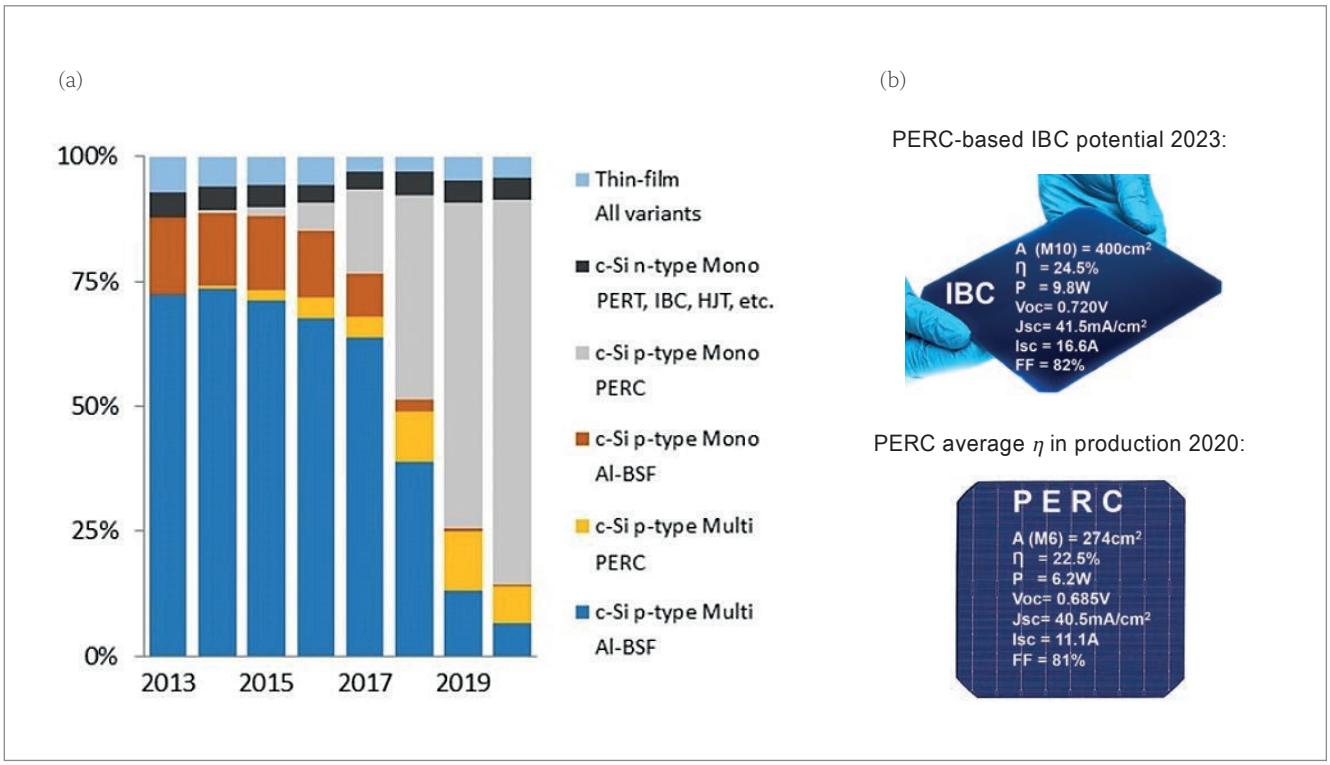

Figure 2. (a) PV solar cell technology market share [3]. (b) Interdigitated back-contact (IBC) potential in 2023 (top) and PERC average efficiency in 2020 (bottom).

and TOPCon, however, and claiming that n-type bifacial is the future.

The situation right now is that Al-BSF has completely disappeared from the scene (for the most part, only India is still building on Al-BSF mc-Si technology). PERC currently dominates the PV market (Fig. 2(a), grey bar), but n-type technologies are today gaining momentum. PERC, with 22–22.5% efficiencies on average in production, is getting close to its efficiency limits, however, and it is becoming much easier to implement new technologies, such as poly-Si on n-type cells, because of technological reasons. Furthermore, the benefits of passivating contacts are greater for n-type cells, as the contribution of bulk recombination is lower than in p-type devices.

In an attempt to prolong p-type's dominance of the PV market, LONGi has two more aces up its sleeve: 1) improved p-type material quality through Ga doping instead of B doping, and 2) increased wafer size. Ga doping has the advantage that there is no light-induced degradation (LID) in p-type material, since the phenomenon occurs as a result of the formation of B–O complexes. This brings the quality of p-type material closer to that of n-type; however, n-type still has its advantages, since it is less sensitive to prominent metallic impurities (such as Fe) and also less sensitive to degradation due to high-temperature processing. Increasing the wafer size from the long-time standard M0 (156×156mm²) to M2 (156.75×156.75mm²) or M6 (166×166mm²), or even up to M10 (182×182mm²) and M12 (210×210mm²), has two major drivers:

"As PERC approaches its efficiency limits, further cost reduction per Wp of cell production will not be possible by efficiency increases alone."

1. As PERC approaches its efficiency limits, further cost reduction per Wp of cell production will not be possible by efficiency increases alone. A cost reduction can therefore only be achieved by increasing the wafer size, which enhances production throughput (in Wp).

2. More importantly, because the big players are able to dictate the wafer size, they can 'wash out' the small producers, which cannot afford to upgrade their production lines to larger wafer formats so easily. At the moment, the 'wafer size war' is being fought mainly by two companies: LONGi, which is promoting M10 (182×182mm²) as standard, and Zhonghuan Semiconductor, which is promoting M12 [5].

Solar cell technology: status and future

Fig. 3 shows the history and possible future of c-Si wafer formats. In 2015 the market was still dominated by M0 formats, with cells having three to five busbars. Today, the average wafer size of newly installed manufacturing lines is M6, with a greater number of busbars. As the cell size increases, the use of half-cut cells is becoming standard in order to avoid increases in resistive power losses due to the higher currents delivered by the larger cells. A perfect shape for a solar cell is

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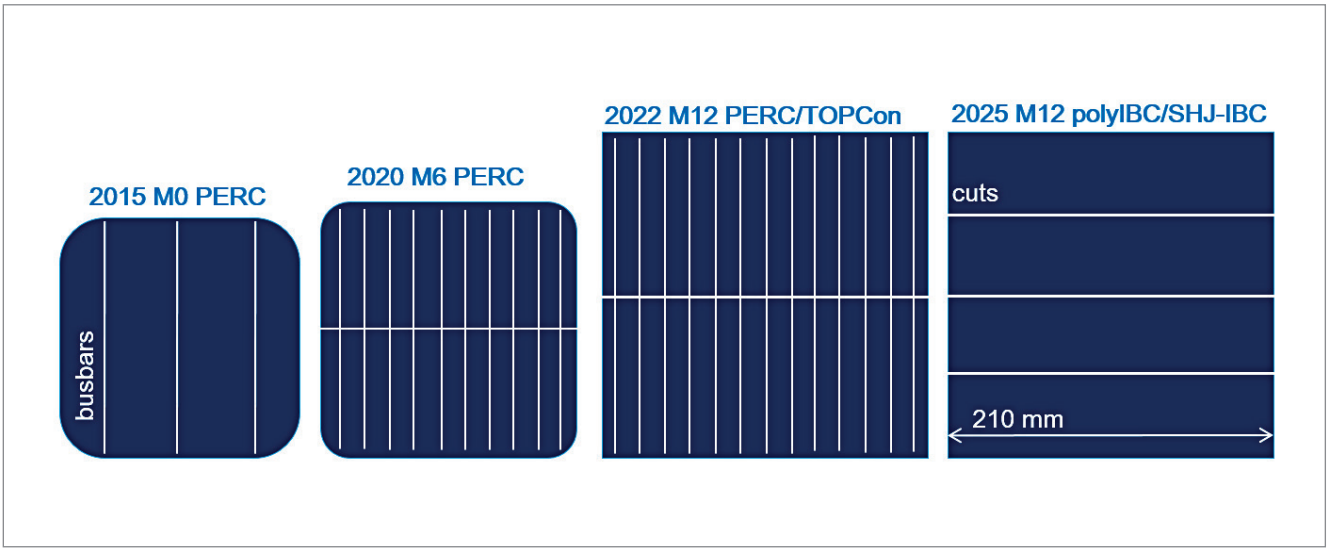

Figure 3. Increasing wafer sizes and number of busbars/vertical lines, and solar cells moving away from being a square (half-cut or more cuts/ horizontal lines).

not a square but rather a rectangle, resulting from cutting the wafer in half (or into even more stripes). In 2022 M12 will become the cell size standard.

A little further in the future, around 2025, the authors believe that back-contact technology will begin to dominate the market, because of its higher efficiency potential (on comparable substrate sizes). The losses from shading on the front side of the cell are eliminated by moving the metallization to the rear, where alternative contacting approaches, such as fully poly-Si passivating contacts, can be implemented without the loss in parasitic absorption. In consequence, interdigitated back-contact (IBC) technology is a highly fancied candidate to win the c-Si solar cell development race. Looking even further ahead, in order to increase efficiencies above 30%, c-Si-based tandem technologies, such as perovskite/IBC tandems [6], will enter the PV arena. For utility-scale applications, these tandem cell architectures will also have to be bifacial.

In this paper, a nomenclature for PV devices analogous to that for the mobile networks will be used. In the past, 3G was the network standard, which today has almost everywhere been replaced by 4G. 3G can be compared to the phase-out of Al-BSF technology, with voltages of around 660mV, while 4G technology can be compared to standard PERC without passivating contacts, having voltages of around 680mV. Currently, 5G is starting to penetrate the mobile network market; this can be compared to c-Si technology using passivating contacts for technologies such as silicon heterojunction (SHJ), poly-Si PERT (TOPCon) and poly-Si IBC, with voltages well in excess of 700mV. 6G represents future tandem solar cells.

It is important to note that all three networks 4G, 5G and 6G will be coexisting, and will be used depending on the particular application and the

"To increase efficiencies above 30%, c-Si-based tandem technologies will enter the PV arena."

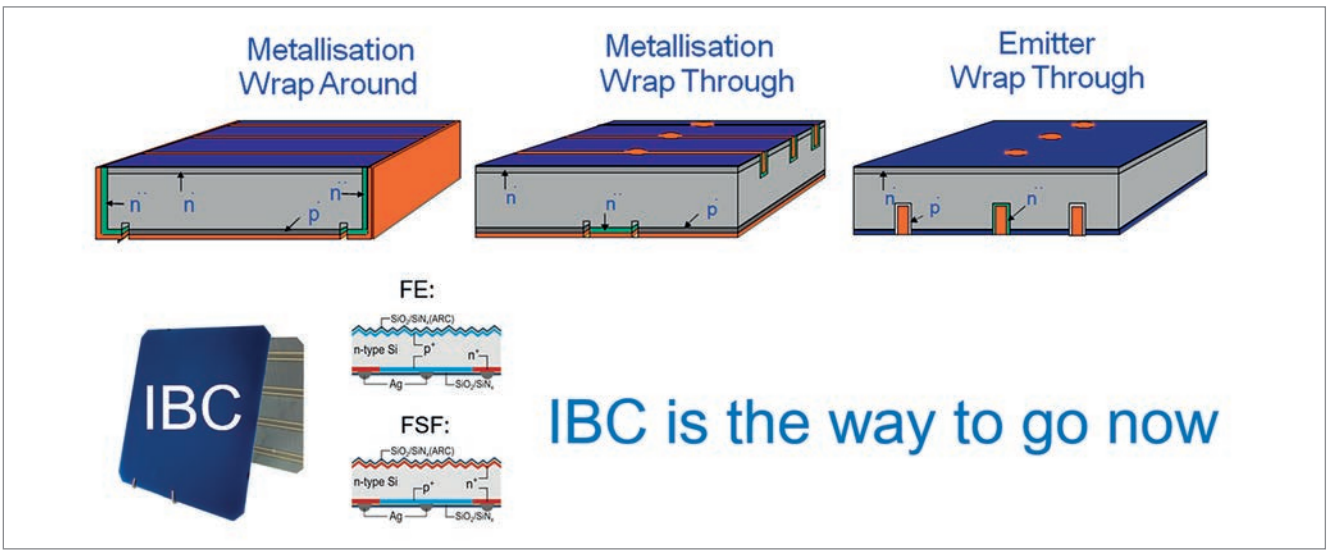

Figure 4. Different geometries of various back-contact solar cell concepts [7].

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population density: it is not necessary to use more costly 5G when 4G is sufficient. The IBC solar cell market has 4G and 5G in production by various companies (which will be discussed later).

Rear-contact technologies

A variety of concepts have been developed in the past by different companies with the aim of bringing back-contact solar cells to the PV market. SunPower, for example, has been producing high-priced IBC solar cells for several decades. However, a number of companies – such as BP Solar and Solland – wanted to establish lower-cost back-contact technologies on the market, such as metallization wrap around (MWA) and metallization wrap through (MWT), as well as emitter wrap through (EWT), as illustrated in Fig. 4.

The only concept besides IBC that has been implemented successfully and launched on the PV market, and which is still in PV production, is MWT from, for example, Sunrise and Sunport Power. However, as in the case of PERC, the average efficiency is limited to values below 23%, when passivating contacts are not used. The implementation of passivating contacts in a p-type concept is much more complicated than in n-type; it is easier to make and contact phosphorus-doped poly-Si, but for p-type two-sided contacted cells, as with PERC, this has to be done selectively at the front, which is a complex process. Then, if the p-type material quality is good enough (>1ms minority-carrier lifetime), p-IBC can be considered. This is what the consortium consisting of centrotherm, FhG ISE, ISFH and ISC Konstanz is doing within the framework of the German project POPEI (poly-Si PERC-based IBC). If successful, POPEI could be the next big thing after PERC.

IBC technologies

Why is the time right for IBC solar cells? Because in order to increase average cell efficiencies above 23% in production, 'classical' PERC technology will in any case have to be replaced. To maintain the cost effectiveness of IBC technology, the equipment developed for diffusions, passivation and metallization will need to be PERC based however. This can be done either with POPEI or with n-type-based IBC processes, as described in Table 1.

Table 1 shows four different IBC technologies on the PV market – two 4G and two 5G using passivating contacts. Furthermore, SHJ producers, such as REC and Meyer Burger, have 5G SHJ IBC technology on their roadmap in the coming years.

ZEBRA from ISC Konstanz, produced by SPIC in Xining, China, with an IBC from Jolywood, is still 4G/PERC based, producing efficiencies up to 24%, with V_{oc} around 700mV. The only equipment which is not used in PERC but used in ZEBRA is the BBr_3 tube furnace diffusion; in addition to that diffusion, Jolywood uses P implantation in order to keep the process single sided.

One of the greatest benefits associated with these 4G technologies is that because they are closely related to the PERC process, PERC technology is not a moving target, relatively speaking, as these IBC technologies can be considered moving with it. This is why the cost of ownership (COO) of these IBC cells is less than twice the COO of PERC. The major differences are still the n-type substrate costs and Ag paste consumption. The 5G technologies from LG electronics and SunPower are rather complex, both using (for example) passivating contact technology, and SunPower using plating in addition. The number of steps and the complexity involved, as well as the use of non-standard equipment, result in very high efficiencies on the one hand, but in high costs on the other; to the authors' knowledge, the cost works out to be more than three to four times that of standard PERC.

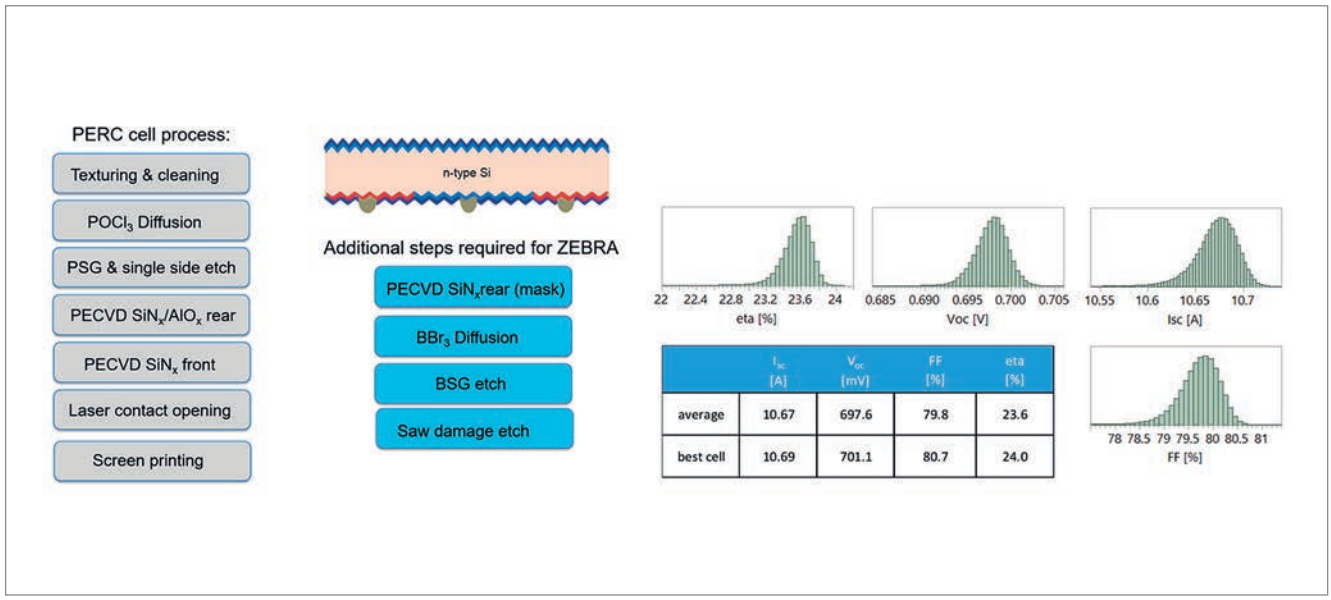
PERC-based IBC technology – ZEBRA

The c-Si PV future belongs to PERC-based IBCs on n-type substrates, potentially with a p-type Cz-Si step in between, when Ga-doping p-type Cz with higher minority-charge carrier lifetimes is considered (in this case poly-Si PERC IBC is also possible). However, the final goal is to achieve efficiencies of 25%+, which will only be possible with '5G n-type IBC technology'.

> "The final goal is to achieve efficiencies of 25%+, which will only be possible with '5G n-type IBC technology'."

SPIC (ZEBRA)	Jolywood	LG Electronics	Maxeon (SunPower)
4G	4G	5G	5G
21.3% [8] Bifacial	Unknown Monofacial	22% [8] Monofacial	22.6% [8] Monofacial
#4 module [8]		#2 module [8]	#1 module [8]
90% PERC related	80% PERC related	Passivating contacts	Passivating contacts
BBr_3 diffusion	BBr_3 diffusion + P implantation	Complex process	Complex process
Processes benefit from PERC improvements		Processes very different from PERC	
COO < 2× PERC		COO > 3–4× PERC	

Table 1. Properties and module efficiencies of four different 4G and 5G IBC technologies available on the market today [8].



	Isc [A]	Voc [mV]	FF [%]	eta [%]
average	10.67	697.6	79.8	23.6
best cell	10.69	701.1	80.7	24.0

Figure 5. PERC process flow, additional ZEBRA steps and results for mass production at SPIC in Xining, China [9].

Advantage	Challenge
High-efficiency bifacial cell	Low-cost n-type wafer
Low degradation	Poly-Si depositions
Low temperature coefficient	Ag consumption
>>> High kWh/kWp	>>> Higher COO, as for PERC

Table 2. Advantages and challenges of PERC-based IBC cell technology.

ISC Konstanz has chosen a method that only one other company, Jolywood, is following as well: 4G IBC without passivating contacts, which nevertheless still yields efficiencies of up to 24%, with voltages above 700mV. TOPCon manufacturers, such as REC and Jinko, implement passivating contacts first into nPERT and have plans to move to passivating contacts for IBC in the future. In the case of ZEBRA, the IBC path is taken first, with passivating contacts being implemented in the future. Fig. 5 shows the PERC process flow and additional ZEBRA steps, as well as the results for mass production [9].

In addition to the very lean process for standard PERC, the IBC ZEBRA process needs only four process steps: a plasma-enhanced chemical vapour deposition (PECVD) SiN_x deposition, BBr_3-diffusion, BSG etch and a polish etch (replacing the single-side etch). AlO_x is not needed, as the passivation is achieved by a BSG/SiN_x stack [10]. Nevertheless, such a simple IBC solar cell process leads to 23.6% efficiency on average, with best performing cells at 24%. The advantages and challenges of such PERC-based ZEBRA IBC solar cells are summarized in Table 2.

High efficiency and bifaciality result in the highest module power densities. High-quality n-type Cz-Si material leads to low degradation, and the high voltages to a low temperature coefficient, which together give rise to a much better kWh/kWp performance, as with PERC. To reduce costs, thinner n-type wafers can be used and Ag consumption reduced or even completely replaced by Cu or Al metal pastes.

Module technology: status and future

There are several module technologies available for IBC cells these days, which work very well and have different advantages and drawbacks. Fig. 6(a) shows a bifacial, stringed, half-cut cell ZEBRA module, and Fig. 6(b) shows a monofacial, full-cell module with conductive backsheet (CBS) technology.

Classical stringing

To the authors' knowledge, ZEBRA is the first and only bifacial, stringed, half-cut cell module on the PV market. Stringing technology is well established in PV production, and standard equipment can be modified for single-sided stringing of IBC cells, making it a low-cost upgrade to an existing module production line. Typical module architectures, such as glass–backsheet, glass–glass and frontsheet–backsheet, and even bifacial configurations can be easily realized. Since interconnection ribbons are soldered or attached by electrically conductive adhesive (ECA) only to the cell rear, bowing needs to be overcome, for example by transitioning to half cells.

Adapted stringing

LG and SunPower have both developed specially adapted stringing technologies that address the bowing issue mentioned above. LG uses a multi-ribbon approach, applying a total of 30 flat ribbons to the rear of the cell; contact between cell and ribbon is established only locally at specially raised areas on each finger of the cell metallization. In contrary to that, the interconnection of SunPower cells is not done by soldering ribbons all along the cell width, but instead by soldering a connector to adjacent cell edges; the connector thus only bridges the cell-to-cell gap. The connector is soldered locally

(a) (b)

Figure 6. (a) ZEBRA module with bifacial, stringed half-cut cells. (b) CBS monofacial full-cell module.

to special solder pads to collect the entire cell current. Because of the long current path that has to be bridged by the cell metallization, this technology has been abandoned by SunPower during its move to 6″ wafers.

Conductive backsheet

Specially developed for interconnecting back-contact solar cells [11], CBS technology is based on a dedicated assembly process and module stack. The CBS houses the module circuit on a copper sheet facing the inside and classic backsheet layers on the outside. An extra sheet between cell and copper provides electrical insulation. Contact between cell and CBS is made at local openings in the rear sheet by ECA or solder paste. This low-stress assembly technology based on pick and place was designed for MWT module production. Although perfectly suited to IBC cells, IBC-CBS technology has so far only been demonstrated successfully [12,13] and not yet entered mass production.

Al foil

Al foil-based interconnection is a promising candidate for lead-free, low-cost and low-series -resistance interconnection and well suited to IBC cells. Cell and Al foil are joined by laser welding, with different approaches being taken in research [14,15] and in industry. SunFlex Solar [16], for

> "There are several module technologies available for IBC cells these days, which work very well and have different advantages and drawbacks."

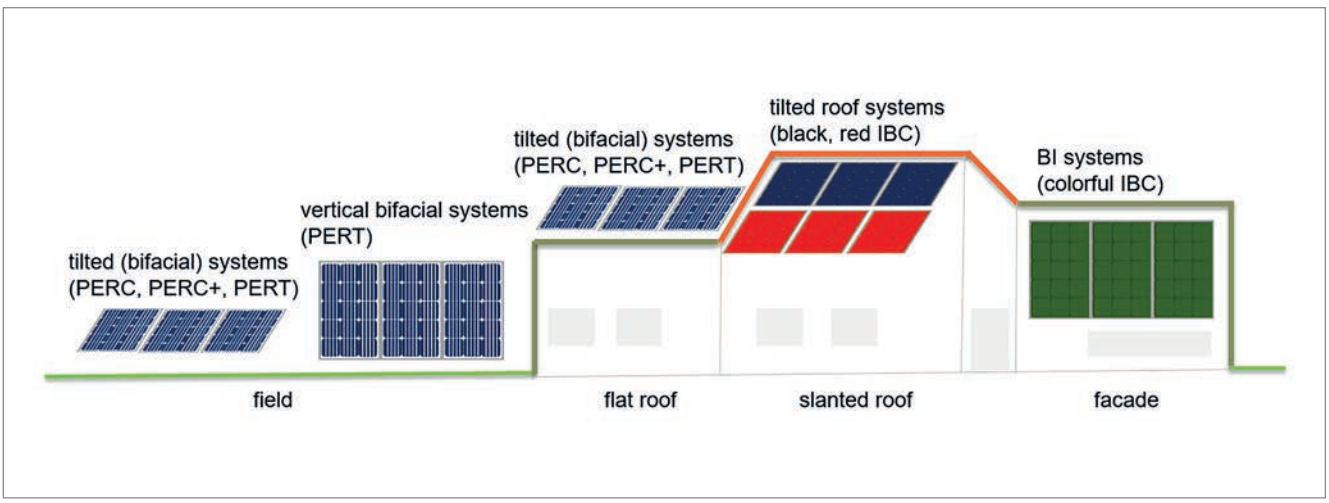


Figure 7. Possible applications of today's IBC modules on rooftops and facades [18].

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example, is developing a solution where an Al circuit similar to CBS is directly laser welded to the solar cell busbars. Recently published patents suggest that SunPower is interconnecting their 6" A-series cells by laser welding, or they are at least carrying out a thorough evaluation of this technology [17].

Applications and market

In 2016 ISC Konstanz published an article in *Photovoltaics International* entitled "Back-contact technology: Will we need it in the future?" [18]. At the time it was already quite obvious that it would be a while before IBC technology would become attractive to the utility-scale market, and that the rooftop, building-integrated PV (BIPV) and product-integrated PV (PIPV) markets would be the most interesting, where IBC has to be implemented initially. Fig. 7 shows the diagram published five years ago, which is still valid today.

The utility-scale market is dominated by PERC and bifacial PERC, with a lower market share held by nPERT (also TOPCon and other passivating contact nPERT). In the rooftop and BIPV market, SHJ (e.g. the REC Alpha Series) and IBC (from, e.g., SunPower, LG electronics, Jolywood and Futura Sun) are becoming more and more visible. The authors are confident that these markets and PIPV will be dominated by IBC architectures in the future.

Fig. 8 presents two prominent examples of BIPV and PIPV. The 2 Degrees Building in Milan with bifacial BiSoN panels [19] is shown in Fig. 8(a); in the future, such buildings will have bifacial ZEBRAs included. Fig. 8(b) shows the Sion car with ZEBRAs implemented in the car body from Sono Motors in partnership with Valoe [20].

Summary and outlook

Back-contact technology in an IBC configuration is the future of PV for the simple reason that it is the technology that every solar cell producer has on its roadmap as the 'final c-Si product' now that c-Si's practical efficiency limit of 26% rapidly approaches. Tier 1 PERC manufacturers, such as Jinko and LONGi, have roadmaps leading to passivating contact nPERT initially and then to IBC structures in two to three years' time. SHJ producers, such as Meyer Burger and REC, have IBC technology on their roadmaps as well. Fig. 9 shows ITRPV's forecast of various technology market shares up to the year 2030.

4G technologies, such as PERC and ZEBRA, might still play an important role, even until 2030; however, they will be step-by-step complemented by 5G technologies with passivating contacts and SHJ. In the authors' opinion, since IBC technology will also be used in the SHJ arena, as well as possibly in the p-type world, the share of IBC will increase much more quickly, as predicted in the graph in Fig. 9; IBC can and will be used in many cell categories. Accordingly, FhG ISE, TNO and ISC Konstanz will organize a revival of the back-contact workshop at the end of 2021 in order to bring the most important players in MWT and IBC technologies together, and to work on the future of back contacts (www.backcontact-workshop.eu).

From 2024 onwards, c-Si-based tandem technologies (6G) are predicted to enter the PV market, also with IBC as a bottom cell for three- and four-terminal devices. The next tandemPV

"Back-contact technology in an IBC configuration is the future."

(a)

(b)

Figure 8. Possible applications for bifacial IBC cells: (a) BIPV project in Milan [19], and (b) PIPV application in a Sono Motors electric car [20].

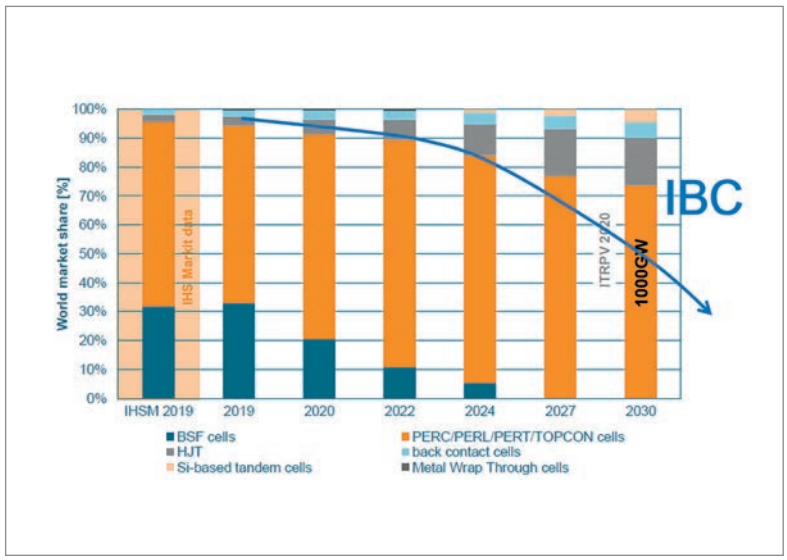

Figure 9. ITRPV's technology market share forecast of solar cell production up to 2030 [21].

workshop will take place in 2021 in Berlin (www.tandemPV-workshop.com). As a result of the first tandemPV2020 workshop in Konstanz, a summary paper was published in *Photovoltaics International* [6], in which it was also described how c-Si IBC cells will play a dominant role within tandem technologies. The future looks very bright for IBC technology – whether it be for p-type or n-type, or for 4G, 5G or 6G. Metal contacts need to go to the back!

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Dr. Radovan Kopecek obtained his Diploma in physics at the University of Stuttgart in 1998. He also studied at Portland State University (Oregon, USA), where he received an MS in 1995, and then in 2002 he finalized his Ph.D. dissertation in Konstanz. One of the founders of ISC Konstanz, he has been working at

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Dr. Florian Buchholz studied chemistry and English at the University of Konstanz and qualified as a high school teacher. In 2016 he defended his Ph.D. thesis on metal surface contamination in c-Si solar cell processing at TUBA Freiberg. He is currently employed as an R&D engineer and project manager at ISC Konstanz, where his main fields of work are the transfer of lab processes to industrial production and the development of advanced passivating contact IBC solar cells.

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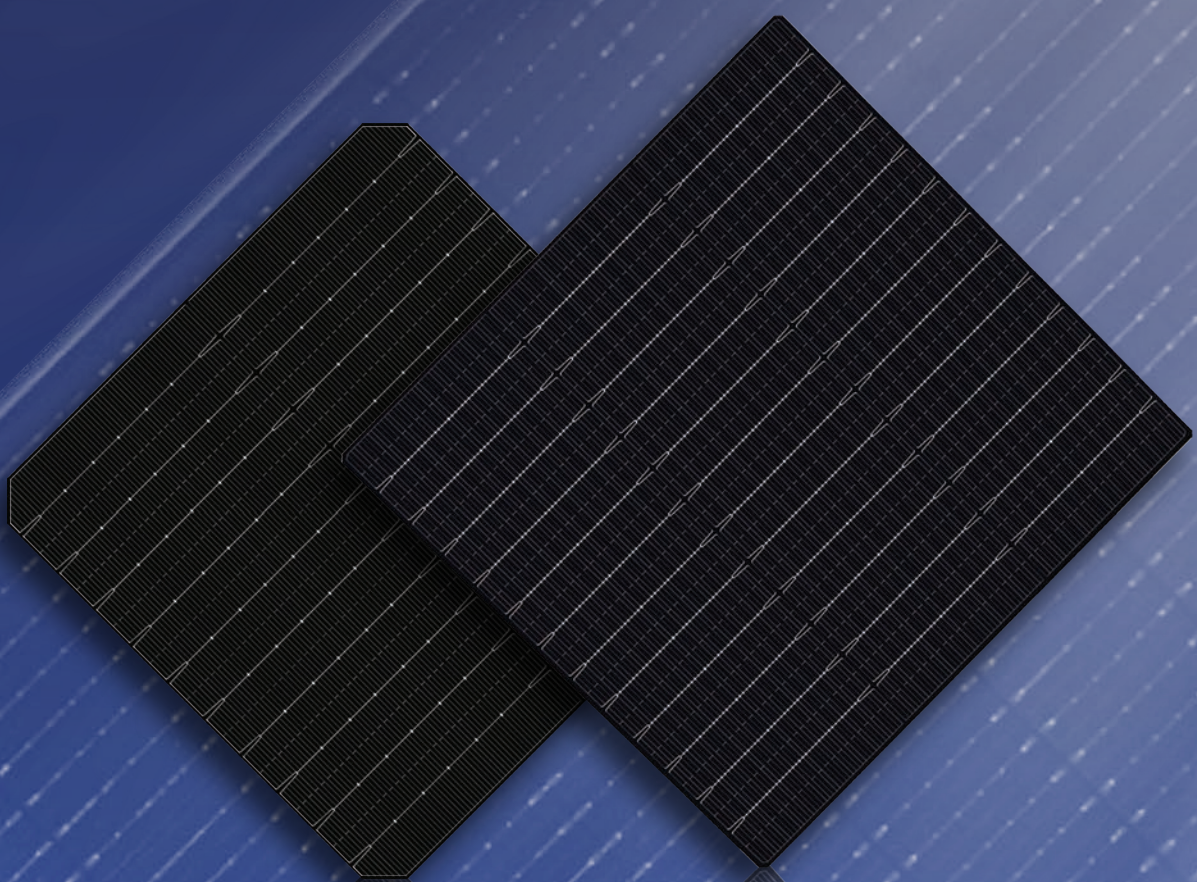

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